Menu name	Subjects	Options	Physically in the set
Personal	Blue Mute	Yes No	Blue mute active in case of no picture detected Noise in case of no picture detected
	Favourite Programmes	Yes No	Favourite program selection enabled Favourite program selection disabled
	Virgin Mode	Yes No	TV starts up once with language selection menu after mains switch on for the first time (virgin mode) TV does not start up once with language selection menu after mains switch on for the first time (virgin mode)
	Standby Toggle	Yes No	Standby toggle activated; by the standby knob the TV is switched to standby and back to normal operation again Standby toggle de-activated
	Auto Store Mode	none PDC-VPS TXT page PDC-VPS-TXT	Autostore mode disabled (not in installation menu) Autostore mode via ATS (PDC/VPS) enabled Autostore mode via ACI enabled Autostore mode via ACI or ATS enabled
	Multipip	Yes No	Multi-PIP enabled Multi-PIP disabled
	Demo Mode Enable	Yes No	Demo mode enable Demo mode disable
	Auto Format Enable	Yes No	Automatic Aspect Ratio detection (black bar detection) software is enabled Automatic Aspect Ratio detection (black bar detection) software is disabled
	Auto Sharpness Enable	Yes No	Automatic sharpness software is enabled (motion compensation depending on noise level) Automatic sharpness software is disabled
	Auto Motion Enable	Yes No	Auto motion software is enabled (smart keys coupled to nexTView) Auto motion software is disabled
	Auto Smart Control	Yes No	Auto smart control software is enabled Auto smart control software is disabled
	Menu animations	Yes No	Animations at start of menu is enabled Animations at start of menu is disabled
Teletext	Cont. Subtitles	Yes No	Continious subtitles enabled Continious subtitles disabled
	TXT Preference	top flof	Preference to top teletext Preference to flof teletext
	Infoline	Yes No	PDC infoline enabled PDC infoline disabled
	East/West Txt	East West	TXT characters for non -/58 set TXT characters for -/58 set

- If an option selection in the Dealer Mode is not displayed, then that is the result of an option selection in the Service Alignment Mode.
- After the option(s) have been changed, they must be stored via the STORE command.
- The new option is only active after the TV is switched off and then back on again using the mains switch (the NVM is then read out again).

8.17 'Option number'

In case the EAROM has to be replaced, all the options will also require resetting. To be certain that the factory settings are reproduced exactly, both option numbers have to be set. These numbers can be found on a sticker on the picture tube.

Menu name	Subjects	Options	Physically in the set
	Video DualScreen	Yes No	Video DualScreen panel present (diagram AC) Video DualScreen panel not present (diagram AC)
Source Selection	SS Type	Euro MD2	Always in MD2
	Euro AV3	Yes No	3rd EURO connector present (diagram K) No 3rd EURO connector present (diagram K)
Audio Repro	Audio Repro	Basic Incr. sound Dolby + eq.	No dolby, no incredible sound, no graphic equalizer (Audio Module no dolby, no incr; diagram O) No dolby, yes incredible sound, no graphic equalizer (Audio Module no dolby with incred; diagram O) Dolby and so also graphic equalizer (Dolby Audio Module; diagram P / P2)
	Cordless Dolby	Yes No	Cordless dolby transmitter module present (diagram AE) Cordless dolby transmitter module not present (diagram AE)
	Dolby Signalling	Yes No	Automatic switching to dolby controlled by broadcaster is present (only software) Automatic switching to dolby controlled by broadcaster is not present (only software)
Miscellaneous	El. Program Guide	Yes No	IC7204 (flash memory) present on TXT+control module (diagram J) IC7204 (flash memory) not present on TXT+control module (diagram J)
	VGA	Yes No	VGA module present (diagram AF) VGA module not present (diagram AF)
	Telephone link	Yes No	Telephone interface panel present (diagram AJ) Telephone interface panel not present (diagram AJ)
	Heatsink Present	Yes No	Heatsinks present on CRT+scavem panel (diagram E) Heatsinks not present on CRT+scavem panel (diagram E)
	Philips logo	Yes No	Philips logo in Virgin mode and Demo mode (only software) No philips logo in Virgin mode and Demo mode (only software)

- If an option selection in the Service Alignment Mode is displayed in black letters, then that is the result of a different option selection in the Service Alignment Mode.
- After the option(s) have been changed, they can be stored via the STORE command.
- The new option is only active after the TV is switched off and then back on again using the mains switch (the NVM is then read out again).

8.16.2 Options in the Dealer Mode

Menu name	Subjects	Options	Physically in the set
Picture	Sharpness in menu	Yes No	Sharpness in picture menu Sharpness not in picture menu
	Tint in menu	Yes No	Tint (normal warm cool) in picture menu Tint (normal warm cool) not in picture menu
	CTI	Yes No	CTI enabled CTI disabled
	Subtitle Squeeze	Yes No	Subtitle squeeze enabled (moves subtitles upwards in case they would fall of the screen) Subtitle squeeze disabled
	Digital Options	100 Hz Digital Scan Natural Motion Nat. Motion Demo Split Screen	Only 100Hz is possible Only 100Hz and Digital scan is possible 100Hz and Digital scan and Natural motion is possible Demo mode; active areas are coloured in a black and white picture Demo mode; lower part is digital scan + natural motion / upper part is only digital scan

Ciruit description

9.1.4 Through-starting via self-oscillation (from the 2nd 50Hz cycle up to take over by the control loop) (Fig. 9.2)

Self-oscillation takes place as long as the secondary voltages are still not too low in order to allow the control circuit to work (so that it can still not be adjusted back).

- Immediately after starting up a linear increasing current flows through primary winding 5-1 which can never be higher than hfe x Ib.
- At the moment that this point is reached the primary winding 5-1 will hold its voltage as a result of which the impedance of the primary coil will start to drop. As a result of this the voltage over primary winding 5-1 and over the positive feedback winding 8-7 drops. The positive feedback current, the base and, as a result of this, the collector current of switching transistor TS7302 also drop, resulting in this starting to reverse.
  As a result of this pin 8 of the positive feedback winding becomes negative. The base voltage of TS7302 drops, the collector voltage increases, the positive feedback winding and the base voltage become more negative as a result of which TS7302 reverses more quickly (once again an avalanche effect, but now in reverse).
- Now that TS7302 is reversed, all energy which was stored in the transformer is supplied to the load. Because the secondary flows want to and can continue to flow (secondary diodes are conducting), the voltages reverse over the secondary windings and as a result of this the voltages over the primary windings also reverse. As a result of this the capacity on pin 5 of the transformer can charge up C2305 to the peak value of 900V (300V + (Vsec x n)).
- At the moment that all energy has been transferred from the transformer to the load, a resonance takes place between the primary winding 5-1 and C2305.
- If, during the resonance, the voltage over the primary winding 5-1 becomes positive, the voltage on the positive feedback winding 8-7 will also become positive. As a result of this the switching transistor will again start to conduct. This results in the voltage on the positive feedback winding 8-7 becoming high and the switching transistor again starts to conduct.
- This process repeats itself as a result of which the secondary voltages are built up more and more until the control loop, which provides the stabilization of the SOPS, comes into operation (see pulse width controller).

N.B.:

- Self-oscillation can also take place if the control circuit is faulty.
- Disconnecting pin 5 of the opto-coupler IC7301 and then carefully increasing the mains voltage using the VARIAC can be handy for fault tracing. As a result of this the SOPS is forced to continue running in self-oscillating mode.

9.1.5 Building up and maintaining the -5V on pin 7 of the transformer (continuous process) (Fig. 9.2)

In order to be able to quickly switch off switching transistor TS7302 and thus avoid its dissipation, -5V is applied to the base of TS7302 when switching off. The stabilization of pin 7 of the transformer is explained here.

- When switching transistor TS7302 is conducting, pin 8 of the transformer has +12V. Because *68328 and D6327 now* start to conduct, energy can be passed on from the source to the load. The output voltage over R3305 is stabilized exactly at -5V by the Zener -(5V6-0V6) via the 5V6 Zener and D6328 and the 0V6 of the BE of TS7300. R3343 and R3337 limit the current through transistor TS7300.
- During the reversal of switching transistor TS7302 the voltage on pin 8 of the transformer drops to -36V. D6327 and D6326 reverse and energy is no longer delivered to the load.

9.1.6 Stopping switching transistor TS7302 from conducting (Fig. 9.3)

The amount of energy which has to be pumped into the transformer has to be determined by the amount of energy which the load requires. In order to control this the pulse width controller on the secondary side makes the photo-diode in the opto-coupler conduct at just the right moment, as a result of which the switching transistor is ultimately reversed. This works as follows:
If the photo-diode on the secondary side starts to conduct, the photo-transistor on the primary side of the opto-coupler also conducts. As a result of this TS7310 starts to conduct, causing TS7311 to conduct. As a result of this the base of switching transistor TS7302 becomes connected to -5V via L5302 and R3306. A short and simultaneously very strong negative base current then flows as a result of which TS7302 reverses quickly and dissipates as little as possible. The quick 'drawing empty' of a transistor with a negative base current is called 'hollowing'.
During the reversal of switching transformer TS7302 there is a positive pulse on pin 5 and, due to this, also on pin 9 of the transformer. During this positive pulse TS7304 conducts as a result of which it is ensured that TS7310 and thus TS7311 also remain conducting. As a result of this TS7302 definitely remains in reverse when the high voltage is present on its collector.
Diodes D6305 and D6333 serve to protect transistors TS7304 and the opto-coupler.

9.1.7 Pulse width controller (Fig. 9.3)

Switching transistor reversed, energy to the load
As long as switching transistor TS7302 is reversed there is a negative pulse on pin 12 and pin 14 of the transformer.
The negative pulse on pin 14 charges C2312 negatively via D6315 and R3317 *(negative charging current I_A)*. As a result of this TS7305 reverses and no current flows through the diode of the opto-coupler. The secondary windings now deliver energy to the load.

Switching transistor conducts, energy in the transformer
As soon as all energy has been passed from the transformer to the load (secondary flow then becomes zero) the polarity of the voltages on the transformer reverses (see self-oscillation). Switching transistor TS7302 now starts to conduct and on pins 12 and 14 of the transformer there is now a positive voltage and on pin 22 a constant negative voltage.

Two current routes are created:
- Because pin 12 of the transformer is positive, D6313 and D6314 conduct and C2312 is charged up positively from its negative voltage (*positive charging current I_B*).
- The +16V output voltage is measured directly via TS7303. Because the voltage on pin 22 is now negative D6318 does not conduct as a result of which the base of TS7303 forms a direct reflection of the +16V output voltage via R3310, R3311 and R3312. For example, with an increase of the +16V the base will increase less than the emitter of TS7303, as a result of which TS7303 conducts more and thus generates a larger current (*positive charging current I_C*). Therefore, using R3311 the output voltage can be adjusted to +16V (so long as the switching transistor TS7302 reverses, pin 22 of the transformer is positive, D6318 conducts and the base of TS7303 lifts. Therefore this control only works as long as switching transistor TS7303 is conducting).

These two positive charging currents charge C2312 positively. As soon as the voltage on the base of TS7305 becomes higher than 1V2 TS7305, starts to conduct. The diodes and, due to these, the photo-transistor of the opto-coupler, conduct, as a result of which switching transistor TS7302 starts to reverse.

Load increase
With increasing load, the +17V and the -17V drop:
- Because the +17V wants to drop the base of TS7303 will want to drop by approximately half with regard to the drop of the emitter of TS7303. As a result of this TS7303 is driven less open, resulting in the *positive charging current I_C* decreasing.
- Because the negative pulse of pin 14 decreases when the output voltages are dropping, the *negative charging current I_A* will also decrease. However, due to the TS7303 control the power supply is correct immediately, as a result of which more energy is pumped into the transformer. As a result of this pin 14 again becomes more negative, causing the *negative charging current I_A* to increase again.
- The *positive charging current I_B* will remain constant because that is only related to the level of the primary voltage 300V (see mains voltage variations).

Due to the increased negative charging current I_A, C2312 becomes charged up more negatively and due to the decreased positive charging current I_C, C2312 will be charged up less quickly. Due to these two mechanisms it takes longer before C2312 reaches the 1V2, as a result of which TS7305 is switched later. As a result of this the switching transistor is switched off later and more energy is pumped into the transformer. As a result of this the load increase is compensated.

Mains voltage variations
When the mains voltage becomes lower, the positive voltage on pin 12 also becomes lower (thus lower than 10V). As a result of this the positive charging current I_B becomes smaller, as a result of which it takes longer before C2312 reaches the 1V2.

When the mains voltage becomes higher, the positive voltage on pin 12 becomes higher as a result of which C2312 charges up more quickly. As a result of this the duty-cycle reduces (T-on becomes shorter if T-off remains the same). In order to limit this duty-cycle when the mains voltage becomes too high the current path I_B receives and additional current path via Zener diode D6321 when the input voltage is too high. In this way there is an additional charge on C2312, as a result of which this charges up more quickly and the switching transistor switches off more quickly. The maximum duty-cycle is limited in this way so that the maximum power in the event of over-voltage can not then become greater than for nominal voltage.

9.1.8 *Standby (Fig. 9.3)*

If the set is switched to standby the 'St-By-INFO' is set low by the standby-µP (active low). As a result of this TS7312 reverses in standby, as a result of which TS7306 conducts via the +5STANDBY supply voltage, R3341 and D6317. Therefore, the diode of the opto-coupler conducts continuously in standby and the 'Audio power Supply' is completely adjusted back to 0V output voltage. In standby the photo-diode continues to be supplied by the +5STANDBY via D6316.

9.1.9 *Protections (Fig. 9.3)*

When a fault is detected on the 4 x 15W sound power amplifier panel, for example because the +16V or the -16V is too low or too high), this panel makes the 'DC PROT' line high (+5V). As a result of this TS7306 will conduct and adjust the power supply completely back (same principle as in standby).
D6316 ensures at the same time that switching transistor TS7302 does not become faulty if the positive voltage is not present on pin 12. The photo-diode is then supplied with the +5STANDBY.
As long as the +17V is greater than 19V4 then, via D6311, R3318, D6331 and D6308, transistor TS7306 will conduct and the power supply will be adjusted back to 0V.

9.2 Changes to the power supply section of the large signal panel

9.2.1 *Semi-standby mode*

For the main supply on the large signal panel it is the intention that in certain conditions the set can be placed in the semi-standby mode, for example as in EPG mode. This means that the power supply works completely but that the series switch is switched off so that the line stage does not operate. The switching on or off of the series switch takes place from the SSP panel via the 'SLOW DOWN' line. This semi-standby principle existed already in MD2.1 (i.e. when starting up the set the series switch must initially be open), but for MD2.2 there are a number of changes which have been made in the power supply section.

	TS7302 conducts, therefore energy into the transformer	**TS7302 reverses, thus energy to the load**	
C2312	positive charging current	negative charging current	
I_A as a result of U_{sec}	0	present	U_{sec} I_A C2312 charged up less negatively
I_B as a result of U_{prim}	present	0	U_{prim} , I_B , C2312 charged up positively more quickly
I_C as a result of U_{sec}	present	0	U_{sec} I_C C2312 charged up positively less quickly

9.2.2 *Degaussing circuit (only for EPG)*

Principle
When changing over from standby to semi-standby in the EPG mode then the degaussing will not work correctly because people can be frightened by unexpected degaussing. To avoid this the degaussing may only take place if the mains voltage is switched off completely and then back on again. For this purpose the control of TS7507 is adapted for sets with EPG.

Operation
When switching on the degaussing switch, TS7505 is triggered via winding 5-6 of the transformer L5550 and TS7515 so that the degaussing can start. C2514 changes up via R3532. When, after this, C2514 is sufficiently charged up (this is determined by D6514), TS7513 and, as a result of this TS7514, will start to conduct. Once TS7514 is fully conducting, TS7512 will continue to conduct and, as a result of this, TS7514 will again continue to conduct (TS7512 and TS7514 together form a thyristor function) until the mains voltage is completely switched off.
Because TS7512 now remains conducting, the base of TS7515 remains high so that this continues to be reversed, with the result that TS7507 remains switched off until the mains voltage is completely switched off.
The number of windings on the transformer is increased so that even in standby the 'thyristor' TS7512-TS7514 remains operational. As a result of this, switching the degaussing back on is only possible after C2514 is sufficiently charged up, in other words after switching off the set.

9.2.3 *Changes to the primary side for reduced standby power (only for MC44604) (Fig. 9.4)*

Introduction
In order to reduce the dissipated power in standby (without degaussing) (< 2W) a new control IC has been selected, namely the MC44604 instead of the MC44603 (the power supply with the MC44603 consumed 3.75W in standby). This new IC has an integrated 'optimalized standby function'.

Higher burst frequency (the number of burst periods per unit of time)
In order to reduce the dissipated standby power the under-voltage level of IC7520 is increased only in the standby mode, as a result of which the burst frequency (the number of burst periods per unit of time) is increased. This is done as follows:
In standby the Vcc of IC7520 increases via R3528 to the level Vth. As soon as Vth is reached the IC starts operating and generates control pulses. The power supply will now start up. Because the start-up circuit is unable to deliver sufficient current, the Vcc is normally taken over by the take-over winding 9-8 of the transformer. However, in stand-by mode the power supply is adjusted back so much that the take over is insufficient and the Vcc sinks immediately. As soon as the Vcc arrives below the under-voltage level the IC, and thus the power supply, will be switched off again and the Vcc will increase via R3528. Because with the MC44604 the under-voltage level is increased only in the standby mode, the number of burst periods is increased per unit of time. The frequency at which the power supply tries to start up during the burst is the same as that of the MC44603 and the same as that in normal operation (the power supply is an FFS (Fixed frequency Supply), in other words it also runs at approximately 40 kHz in standby mode).

Other changes to the primary side for reduced standby power for the MC44604
- R3528 is increased for the MC44604 as a result of which the dissipation in this resistor is smaller. In order to ensure that the start-up time is the same as before the C2525 is smaller for the MC44604.
- Because the C2533 (voltage on pin 11 determines the duty-cycle) is smaller for the MC44604, the duty-cycle is built up more quickly as a result of which the slow-start runs more quickly. As a result of this the burst period (the time that the power supply tries to start up in standby) is shorter, as a result of which the power supply itself works more efficiently (less dissipation losses in the power supply itself).

9.2.4 *Changes to the secondary side for the reduced standby power (only for MC44604) (Fig. 9.5)*

Place MC44604 in standby mode
The MC44604 must receive a sign in order to enter the standby mode with reduced burst frequency. Pin 15 of IC7520 is used for this. As soon as the input current on pin 15 is greater than 35 mA then IC activates its standby mode.
In order to create this current surge a change has been made to the secondary side of the main power supply. When the STANDBY signal is low (active), TS7589 will reverse as a result of which the full +5STANDBY power supply suddenly arrives on the positive side of C2590. C2590 is unable to follow this rapid change and drives TS7588 into full conductance as a result of which a large, brief current starts to flow through the photo-diode of TS7556 (opto-coupler). As a result of this a brief, strong current peak which flows to pin 15 of IC 7520, is generated on the primary side and the MC44604 activates its standby mode.

Maintaining power supply in standby mode for a power supply with the MC44604
Because C2590 charges itself up as soon as the standby mode is activated, at a given moment TS7588 will start to reverse. Because TS7591 only conducts continuously in standby mode (only in the standby mode is the +5STANDBY power supply on the base of TS7591 via R3586 and R3598), a current can only still flow through the diode of the opto-coupler via D6592 and TS7591 to earth. This current is large enough to maintain the standby state. Because TS7591 also conducts during the 'burst' (the time that the power supply tries to start up in standby) the power supply is adjusted back even harder during the 'burst'. As a result of this the 'burst' will not last as long.

Stable +5STANDBY with the MC44604
In order to prevent that the +5STANDBY becomes too low in standby mode as soon as the input voltage of the voltage stabilizer IC7560 is at the lowest point (as a result of which even a POR could be generated), a few changes have been implemented for the power supply with the MC44604:
- Due to the higher burst frequency the ripple on the 5STANDBY is smaller. As a result of this the smoothing capacitor C2571 can be smaller.
- D6561 has been replaced by a type with a low forward voltage (0V2), as a result of which less voltage loss occurs.
- The transformer has been examined again in order to obtain improved efficiency in standby mode.

In this way it is ensured that the input voltage of the voltage stabilizer IC7560 is always large enough to create the +5STANDBY.

Changes for normal operation with the MC44604

- D6550 is added to protect the power supply if the +5STANDBY fails. If the +5STANDBY fails, the STAND-BY signal drops out as a result of which TS7592 starts to reverse. As a result of this thyristor TH7590 starts to conduct as a result of which the voltage over C2561 and C2571 will become too high. Zener D6550 has been added in order to protect these capacitors. At the same time this Zener ensures that the power supply is adjusted back to its maximum. The power supply will start up again, be adjusted by the maximum again, etc.→ hick-up mode.
- Because more energy is demanded from the +8V6 power supply in the MD2.2, the +8V6 voltage stabilizer IC7569 is a type which only requires low over-voltage in order to be able to generate a stable +8V6 (a so-called 'low drop' type).

9.2.5 Primary over-voltage for the MC44604 (Fig. 9.4)

Over-voltage detection for the MC44604
For the MC44603, over-voltage detection takes place via the Vcc input of the IC. In the MD2.2 for an MC44604 the separate OVP input is used on pin 6 of the IC. Since the Vcc depends too much on the mains voltage (+300V DC) and the load, it is possible that at high load large peaks arrive on Vcc as a result of which the OVP is triggered. Therefore, the voltage on winding 9-8 of the transformer is detected via a clamp circuit and a divider (D6548, R3548 and R3549). Only if pin 6 becomes higher than 2V5 will the power supply go into protection (hick-up mode).

Operation at increased input voltage (+300V DC)
In order to obtain a more constant output power as a function of the mains voltage, R3529 is added between the +330V DC and the current sense pin 7 of the IC. This sets a DC component which is dependent on the level of the +300V DC on the current sense input at the top of the current sense voltage, such as that which is measured on the source of the TS7541 FET-link. As soon as the +300V DC increases the complete current sense signal is raised a little on pin 7 as a result of which the T-on decreases by a constant value.

Video processing

9.3 PALplus (fig. 9.6)

9.3.1 Introduction

With 16/9 sets, the PALplus module takes care of both the vertical conversion and also the improved separation between luminance and chrominance.
The module receives the 8 bit Y, 2 bit U and 2 bit V signals from the A/D convertor in the Feature Box. After the PALplus decoding, the signals again go via the AI panel to the Feature Box, where the 50 Hz picture is converted to 100 Hz. Control is provided by the *snertbus* of the processor on the Feature Box. The PALplus module, the AI PCB and the Feature Box are connected by a series of timing signals.

9.3.2 General operation

The MACPACIC (Motion Adaption Colour Plus And Control IC) is controlled by the *snertbus*. The most important
function of this IC is to take care of the separation between luminance and chrominance if MACP is used in the transmitter. The MACPACIC uses both the direct Y, U and V and also those stored in MEM1.
MEM4 is an extra working memory.
The processed picture information is written to memories MEM2 and MEM3.
The VERIC (Vertical Reconstruction IC) reads Y, U and V from memories MEM2 and MEM3 and once again makes a picture of 574 lines from the 430 picture lines by means of the 144 helper lines. This IC is monitored by the MACPACIC which generates a number of clock and sync signals for this.
The module input and output are 16 MHz. The module operates at 32 MHz.

9.3.3 Motion Adapter Colour Plus

The MACPACIC sees to separation of chrominance and luminance if MACP (Motion Adaption Colour Plus) is used in the transmitter. Because of this, the picture is free from chrominance and luminance crosstalk.
The first raster is written to memory MEM1. When the second raster is presented directly to the MACPACIC, MEM1 will be read out causing both rasters to be present at the same time at the MACPACIC input.
MACP can be used independently of the picture mode, i.e. also with 4/3 transmissions.

9.3.3.1 Film mode
In the film mode, 50 rasters are made of the 25 pictures in the transmitter. There is no time difference between the successive even and odd rasters. Because of this,
the picture information of line N in the even raster will be nearly identical to that of line N in the following odd raster. The chrominance of line N in the first raster is in phase opposition to the chrominance of line N+312 in the second raster. In the receiver, addition of the even and odd rasters will thus produce a Y signal which is free from chrominance. Because of this, no further suppressions of the chrominance
at 4.43 MHz are required in the Y channel.
After the PAL demodulator, frequencies around the 4.43 MHz in the Y signal give a U and V component which is in phase opposition for the lines N and N+312. Addition of two successive rasters in the U and in the V channels will eliminate this colour component.
These operations are termed FCP (Fixed Colour Plus), which produces the same result as a comb filter.

9.3.3.2 Camera mode
In the camera mode, unlike the film mode, there is a time difference between the successive even and odd rasters. This time difference causes differences in the successive rasters, especially in content, with fast-moving pictures. The aim will always be to switch over to FCP as far as possible since this gives the best picture quality. This is only possible however if there is almost no difference in picture information with the successive rasters.
Accordingly a movement detector is built into the decoder and this determines for each small part of the picture whether any movement is present. Memory MEM4 is used for this.
With pictures where there is little movement, indicated by the movement detector, switchover to FCP occurs.

With fast-moving pictures the bandwidth of the Y signal is limited to 3 MHz, because of which the chrominance is removed at 4.43 MHz. The resulting Y, U and V are written by the MACPACIC to memories MEM2 and MEM3.

9.3.4 *Vertical conversion*

To reproduce a 16/9 picture in a 4/3 format the 574 picture lines are converted to 430 lines in the transmitter. Because of this, picture information is lost, and without correction this leads to reduction in the vertical resolution.
To be able to make good this loss in vertical resolution, the 'lost' Y information is AM modulated on a 4.43 MHz carrier wave with the same phase as the U signal and is processed in the black bars above and below the picture.
The 72 lines in the black bar above the picture contain the 'lost' information of the upper half of the picture. The 'lost' information from the lower half of the picture is to be found in the 72 lines in the black bar below the picture. These lines with modulated 'lost' information are also termed 'helper lines'.
The VERIC will once again make a picture of 574 lines from the 430 picture lines.
A 'reconstruction' takes place for the Y signal, in which use is made of the 144 helper lines. Since no helper signal is present for U and V, these are determined by 'interpolation'.
When the upper half of the picture is processed, the helper lines are routed to MEM2 and the picture to MEM3. For the processing of the lower half of the picture, the picture goes to MEM2 and the helper lines to MEM3.
Writing to these memories is done by the MACPACIC, readout being carried out by the VERIC.
In film mode, a complete picture is present after two rasters and because of this the conversion will take place for each picture.
In camera mode because of the time difference between two successive rasters there is a difference in picture content because of which conversion must be carried out for each raster. The helper lines are then composed differently and the use of the memory will therefore also be different.

9.3.5 *Transparent mode*

With a non-PALplus transmission, luminance and chrominance are switched through in the MACPACIC.
The top and bottom picture halves are routed respectively into memories 2 and 3. The VERIC then sees to it that the information for the even and odd raster is read in the correct way.

9.3.6 *Detection*

To be able to recognise when this extra PALplus information is present in the video signal and to be able to detect and demodulate this correctly, some extra information is also added.

Line 23 therefore contains no picture information but does contain some signalling bits such as:
- camera or film mode
- MACP used
- helper lines present.

These bits are detected by the MACPACIC.
This line also contains a reference burst with the correct amplitude, DC and phase for the helper lines.
Line 623 contains the reference level for white and black.

9.3.7 *Remarks*

With a PALplus set, the chrominance IC TDA9144 is used instead of TDA9141 or TDA9143.
The helper lines with Y information modulated at 4.43 MHz, are demodulated in the PAL demodulator and multiplexed in the Y signal. Since information which comes out below the back level is present here, the blanking in the IC has been adjusted.
The chrominance IC TDA9144 generates line 22 which contains the references for the black level and the DC level of the helper lines. Some filters in the IC, both in the luminance and in the chrominance channel, are if necessary switched off with PALplus.
There is no PALplus recognition within the TDA 9144.
This means that all PALplus functions from the microprocessor must be indicated via I²C.
The microprocessor in turn receives PALplus recognition information from the PALplus module.
The MACPACIC generates the 16 MHz and the 32 MHz clocks. The phase between these two clock signals is adjusted by S5100.
All processing operations in the PALplus module are digital.

9.4 CRT & Scavem

9.4.1 *Power limiting of the RGB amplifiers*

9.4.1.1 *Introduction*

The RGB output amplifiers are identical to those used in the MD 2.1, though in the lowest segment of the MD2.2, the RGB output stages are no longer fitted with heat sinks. To ensure that the dissipated power, which is produced chiefly at high frequencies, remains within the limits of these output stages, an extra circuit is added. In case of consumption greater than 3.6 W (measured via R3373), this circuit will reduce the definition of the picture. This causes the current consumption of the output stages to fall. In practice, this power reduction circuit will only be activated in case of a picture with a great deal of noise.

9.4.1.2 *Circuit*

The power consumed by the output ICs is detected across resistor R3373; this is fed to TS7374. This is an amplifier with an amplification factor of -1.
The collector voltage of TS7374 is thus equal to the voltage measured across R3373.
If the collector voltage of TS7374 rises, then TS7377 will conduct more and the collector voltage of TS7377 falls.
In case of current consumption higher than 18 mA (3.6 W), the collector voltage of TS7374 becomes greater than 6 V, the collector voltage of TS7377 becomes lower than 11.4 V and because of this, TS7338, TS7348 and TS7358 start to conduct.
When these transistors conduct, a capacitance is placed in parallel with the input signal, causing the picture definition to be reduced and the current consumption, and thus the dissipation too, to fall once again.

9.4.2 *Improved SCAVEM*

To improve Scavem operation, a larger current of about 1 A pp is sent through the Scavem coil. To achieve this, the amplification of the output stage is adjusted (R3408 200 ohms instead of 100 ohms) and the output transistors TS7414 and TS7415 are changed to power transistors (BD139, BD140).

Ciruit description

9.5 Luminance Transient Processor (LTP) (fig. 9.7)

9.5.1 Introduction

In the MD2.2, the LTP IC TDA9177 may optionally be added in front of the video control IC TDA4780. This IC is I²C controlled and carries out some corrections to the Y signal. These are:

- smart peaking
- step improvement
- noise suppression

9.5.2 Functional description

9.5.2.1 The input signals

The input signals are formed by YUV on pins 5, 9, 7 and a sandcastle on pin 1. The output signals are YUV on pins 20, 16 and 18. The U and V signals are delayed according to the corrections to the Y signal.

9.5.2.2 Smart peaking

Smart peaking is a circuit which only applies peaking to small signal changes; because of this, details in the picture can be seen more clearly. The extent of peaking and the signal amplitude to which smart peaking operates, can be adjusted via I²C. With large signal amplitudes (e.g. with black-white transitions) there will be less peaking to avoid unwanted shadow effects. When the LTP is used, the software peaking of the Feature Box will be turned off but the hardware amplification continues to operate.

9.5.2.3 Step improvement

This provision ensures than black-white transitions are made even steeper. The result of this is that the picture gives a still sharper impression.

9.5.2.4 Noise suppression

The LIMERIC in the Feature Box determines the noise level in the picture and appraises this by means of the noise figure which is passed on via I²C to the microprocessor. On the basis of the noise figure, in addition to the degree of noise suppression in the LIMERIC and the degree of DNR, the degree of peaking together with the 'steepness' and the 'coring' in the LTP is now also reduced in proportion with the rise in the noise figure. Because of this, even better noise suppression can be arranged.

9.6 Chrominance notch filter

As well as a chrominance-free Y signal, the COMB filter also produces a few unwanted residues in the vicinity of 4.43 MHz. These residues can be clearly seen when there are sharp colour transitions. To suppress this interference, a filter is fitted between the Y output of the COMB filter and the input of the chrominance IC (IC 7352). This filter is switched on together with the COMB filter. As soon as the COMB filter is switched on (COMB ON/OFF is high), TS7396 will then conduct and the LC circuit (C2351, C2352 and L5382) is switched on. This LC circuit gives an extra 6 dB of suppression at 4.43 MHz.

9.7 Transparent OSDs and menus (fig. 9.8)

9.7.1 Introduction

In the first instance, the operating menus of GFL and MD2.1 consisted of a menu block with a background colour and printed on it the menu text in a foreground colour. With the menus of the MD2.2, the menu block with background colour is replaced by a block in which the main picture is displayed attenuated and the menu text is shown in white on it. With the so-called 'Blending' circuit it is possible to display these so-called 'transparent operating menus' on the screen.
To produce these menus, a number of control signals are required, such as the RGB signals and the Fast Blanking. These four signals were hitherto sufficient to be able to display a menu. However, for the transparent operating menus an extra timing signal is required, namely the COR-NOT signal. The signals are now used as follows:

- At the time that the 'menu block' is written, the TXT-IC produces a low on the COR-NOT line. At that time the blending circuit will ensure that if a specified beam current is exceeded, the contrast is reduced via the beam current limitation in the video controller TDA4780. By only reducing the contrast with effect from a specified beam current, darker picture sequences are displayed unaffected so as to prevent these disappearing completely below the black level.
- However, when text is to be displayed in a menu block, the Fast Blanking information is used to switch off the blending circuit again. Because of this, the contrast is not reduced only where the text is shown in white.

9.7.2 Blending circuit

The blending circuit is located on the TXT+control panel.
If we assume in the first instance that there is no menu (COR-NOT line is high), then TS7453 conducts and TS7454 is in the blocking state. Because of this, TS7455 conducts in such a way that TS7457 blocks sufficiently to ensure that the V_{OUT} can follow the V_{BCI} via the BE of TS7459 and the BE of TS7458. At the time the menu appears, the COR-NOT line will become low and TS7454 will conduct. The resistor division R3445 and R3443 now sees to it that the base of TS7455 is set to 2V8.

- As long as V_{BCI} < 2V8, V_{OUT} follows the V_{BCI} via the BE of TS7459 and the BE of TS7458. This applies to the darker picture sequences and so these are not attenuated.
- If a voltage increase to above 2.8 V occurs, the base of TS7455 will only partially rise (due to the voltage division R3443, R3444, R3445). This only partial voltage rise is passed through the BE of TS7455 and the BE of TS7457 to the V_{OUT}. Because of this, the V_{OUT} will rise less strongly only if the V_{BCI} is greater than 2V8 (lighter picture sequences). This results in a reduction in contrast.

In other words, the DC setting of the base of TS7457 governs the changeover point of the contrast reduction (and thus the brightness at which the contrast reduction must begin with transparent menus).

9.7.3 PIP in front of TXT in a set with blending circuit

In a set without transparent OSDs and menus (MD2.1), it is desirable to have the PIP card always in the foreground (and thus in front of the menus, in front of the OSDs and in front of the TXT). This is done in MD2.1 via the TXT-KILL line and TS7518 (in PIP-mode TXT-KILL is high causing the FBL-TXT to be short-circuited (deactivated) via TS7518).
In a set with transparent OSDs and menus (MD2.2), the PIP card is placed in the background so that the PIP card is viewed through the transparent OSDs and manus. Only in the TXT mode is it desirable to have the PIP card in the foreground. For this the circuit round TS7221 has been added to the FBL-TXT line on the TXT+control panel. C2220 is chosen so that TS7221 passes the FBL-TXT signal to the TXT-ENABLE only in the TXT mode and not in any other modes.

- Only in the TXT mode is the FBL-TXT line constantly high so that C2220 is charged and TS7221 conducts constantly. The FBL-TXT is passed to the TXT-ENABLE and therefore with PIP the FBL-TXT is short-circuited via the TXT-KILL (PIP in front of TXT).
- In all other modes (e.g. OSDs, menus and TXT-mixed mode), FBL-TXT is not constantly high. Because of this, C2220 is not sufficiently charged so that TS7221 is constantly in the blocking state. Because of this, the FBL-TXT is not passed to the TXT-ENABLE so that with PIP, the FBL-TXT cannot be short-circuited via the TEXT-KILL (PIP behind OSDs, menus, mixed mode).

9.8 Automatic Aspect Ratio Adaption (AARA)

9.8.1 Introduction

With certain wide picture transmissions, the WSS bit (Wide Screen Signalling bit) is not included with the transmission. This applies to transmissions in 22/9, 16/9 or 14/9 format.
The customer on the reception side is then faced with a picture where the format is not correctly adjusted (black bars). This can then only be corrected by operating the picture format button on the remote control.
AARA now provides automatic adjustment of the picture format.

9.8.2 Operation

The software in the Feature Box contains a 'black bar detection algorithm'. This black bar detection looks to see whether black bars are present at the top or bottom of the picture. This is done by means of the SMARTIC.
If these bars are present for more than 22 seconds then the picture format is corrected to a maximum of 22/9. The picture width is adjusted by the PANIC and the picture height by the PROZONIC/MELZONIC.
Black bar detection operates independently of the operating software of the set.
Black bar detection can be overruled by:

- the WSS bit
- by an external 16/9 status on a scart input
- by adjusting the picture proportions manually

This function is implemented independently by the software in the Feature Box.

Audio processing

9.9 Audio amplifier

9.9.1 Introduction

For the MD2.1 sets we had different versions:

- Non Dolby fighter version
- Non Dolby horn version
- Non Dolby subwoofer version
- Dolby subwoofer version

In order to be able to delivery more audio power, for the most expanded MD2.2 a choice can be made for a separate audio amplifier, the so-called Audio Amplifier module. For this the audio power supply has to be stronger, as a result of which a stronger power supply unit - the so-called 'Audio Power Supply' - is used. As a result of this we have one additional version in the top MD2.2 sets:

- Top Dolby subwoofer version 4 x 15W.

9.9.2 Block diagram of the Dolby subwoofer version (Fig. 9.6)

The audio signals Surround, Left, Right and Centre originate from the Dolby Audio Module. The power of the output amplifier is 15W per channel.
On the LSP the output amplifier in a Top Dolby subwoofer version is only used for amplifying the surround-sound signal. This has the advantage that a separate channel is provided for both L and the R surround. Because the output signal from the amplifiers is at a DC level of +14V, the outputs are AC coupled to the surround loudspeakers.
On the Audio Amplifier Panel the amplifiers are localized for the Left, Right, Centre and Subwoofer signal.

- The signal which is intended for the subwoofer is a mono signal (L and R are added), because the low frequencies are not direction sensitive. The higher frequencies are filtered out from 270 Hz. The DBE circuit which was previously on the LSP, has now been mounted on the Audio Amplifier Panel. This DBE (Dynamic Bass Enhancement) circuit provides an improvement in the low tone reproduction which is supplied to the subwoofer. The lower half of IC7740 is used for amplifying the subwoofer signal.
- The L and R signals are amplified in the 2 upper halves of amplifiers IC7740 and IC7750. The L and R signals both run via a 200 Hz filter to the internal squeeters which provide the stereo effect, or directly to the internal loudspeakers. In the latter case the input of the subwoofer amplifier is also connected to earth.
- The Centre signal runs via a high-pass filter at 310 Hz and the lower half of amplifier IC7750 to the centre speakers at the bottom centre of the set.

The internal or external selection is determined by a switch on the Clickfit Panel.

9.9.3 *Internal/external selection (Fig. 9.10)*

The selection is made using a switch on the Clickfit Panel which sends either +6V or earth to pins 9, 10 and 11 of IC7735.
For the internal mode pins 9 to 11 (inclusive) are set low. As a result of this all switches are in the lowest position.
For the L and R signal which is intended for the squeeters, all frequencies lower than 270 Hz are filtered out first.
Before these signals arrive on the output amplifiers they are initially attenuated by R3700, R3701, R3702 and R3703.
The power supply for these output amplifiers is symmetric (+16V and -16V), as a result of which all outputs can be coupled directly to the loudspeakers. The amplification is determined internally in the output amplifiers by means of 2 internal resistors between the input and the output.
The Boucherot filter consists of C2746, C2776 and R3746 and serves to filter out oscillations at high frequencies.
All amplifiers are almost identical, only the values of the Boucherot filter can vary depending on the type of loudspeaker which is used.
The subwoofer signal is a mono signal and runs via the DBE circuit to the respective output amplifier in the internal position.
In the internal position the subwoofer signal from the output amplifier is connected to earth, as a result of which the subwoofer is switched off. The L and the R signal is sent directly to the output amplifiers.
The centre channel remains operational, irrespective of the position of the INT/EXT switch.

9.9.4 *Mute circuit (Fig. 9.10)*

The sound can be muted in various ways in the output amplifiers:

- When the supply voltage becomes smaller than +6V or -6V, the IC will automatically interrupt its non-inverting input. This IC therefore automatically suppresses unwanted signals when switching on and switching off.
- The mute can also be activated externally (active low) via the AMP-MUTE2 line, which originates from the mP. This mute is switched off by the remote control, blue mute, programme switching, etc.
- When switching on the mains voltage, electrolytic capacitor 2788 forms a brief short-circuit, as a result of which the voltage is held low at point 2, as a result of which the IC is muted. This avoids a plop when switching on.

9.9.5 *Protecting the audio output stage (Fig. 9.10)*

The supply voltage of the output amplifiers is symmetrical (+16V and -16V). Therefore the outputs from the amplifiers are connected directly to the loudspeakers.
Therefore, during normal operation the output signal contains no DC components. C2761 can absorb any small fluctuations.
If one of the supply voltages now becomes too high or too low or if DC components arrive on one of the outputs because, for example, an IC is faulty, then TS7760 or TS7761 will start to conduct. As a result of this a current flows through R3760 which causes TS7762 to conduct.
The DC-PROT / STBY line therefore comes to 5V, as a result of which the Audio Power Supply goes into protection.
If the positive and the negative supply voltages reduce simultaneously, the voltage on C2761 remains at approximately 0V.
On the centre signal there is a DC voltage of approximately 6V, this is on the emitter of TS7767.
When the +16V becomes lower than 11V, TS7767 and thus TS7760 start to conduct and the DC-PROT signal will still be activated.
In stand-by the 16V supply voltage is switched off; the DC voltage on the centre signal is 0V and TS7767 does not conduct. The C AC signal is max. 0.5V and does not influence the circuit.

9.9.6 *DBE circuit*

DBE or 'Dynamic Bass Enhancement' is used in order to obtain an improved lower tone reproduction using the same subwoofer.

- Circuit 1 adds the L and R signals (the subwoofer requires the low information of both signals) and sends this added signal through a low-pass filter. All frequencies higher than 270 Hz are feedback intensely.
- Circuit 2 has a suppression at 70 Hz (90 Hz for Acoustic Horn).
- Circuit 3 has a frequency-dependent feedback. At 60 Hz the feedback resistance, and thus the amplification too is the greatest. D6720 and D6721 form a limiter if the signals one too large. Circuits 2 and 3 together form an amplification of the frequencies around 60 Hz.
- Circuit 4 is an invertor which 'rectifies' the signal again before it goes to the output amplifier of the subwoofer. By using this stage the amplification factor can still be changed if required. At the same time R3728 and C2728 form a filter which truncate all harmonics above 700 Hz which are caused by the DBE circuit.

9.10 Audio path on the Dolby Audio Module for Double Window (Fig. 9.11)

The 'Double Window' feature also has consequences on the audio section. For Double Window it applies that the sound of the main picture (the left picture) always goes to the loudspeakers, while the sound of the second picture (the right picture) goes to the main headphones.
The additional headphone selection takes place by using an additional switch SK4 and TDA9860.
SK4 provides the selection for the various audio sources, while TDA9860 makes the selection between:

- The classic headphones.
- Double Window headphones originating from an external audio source (SK4).
- The mono signal originating from the tuner on the Full Double Window module.

The configuration around SK1 is identical to that of MD2.1 with the difference that in the MD2.1 this switch was mounted on the SSP and all signals required in the MD2.2 are supplied to the Audio Module via a ribbon cable from the SSP, where the switch is now mounted.
Because SK1 is now on the Audio Module, SK4 can now be switched parallel directly here. This HEF provides the selection of the various audio sources for the headphones in Double Window. SK4 is driven by 2 bits of IC7590 which are applied via I^2C.
Both HEF's are supplied with an 8V5 power supply which comes from the SSP.
For SK1 there are two inputs for front: front L/R and front L/L. As a result of this it is possible to place a mono signal, originating from the front, onto both the left-hand and the right-hand channel.

However, SK4 has no automatic answer to both channels for the front input (all inputs are occupied), for a mono front signal only the left-hand loudspeaker will be driven to full power.
This is solved by IC7590. For a mono signal IC7590 places the mono signal on both the left-hand and the right-hand side. IC7590 is a TDA9860 which is also used in the GFL. However, for the MD2.2, 3 functions of the IC are used as additional functions with regard to the GFL (the remaining functions are 1 to 1 identical):

- The selector switch
- The volume control: which can now no longer be executed on MSP3410 because not all audio sources are offered to MSP3410 for the 'Video Dualscreen' headphones.
- The 2 control bits (pin 2, 31) for SK4.

Ultimately the input of IC7590 is sent to the headphones amplifier.

Wireless dolby

9.11 Transmitter (Fig. 9.12)

9.11.1 Block diagram

We can recognise 3 basic blocks in the block diagram of the transmitter:

1 FM transmitter (1403)
The FM transmitter is a screened module which is I^2C controlled by the main-μC of the TV:
   * At program switching the incoming surround sound signal from the Dolby Audio Module is muted (by the dolby IC SAA7710)) to avoid plops in the surround speakers.
   * At switching off the surround mode, first the incoming surround sound signal is muted (to avoid plops) and then the local oscillator in the transmitter is switched off. As the local oscillator is switched off also the 19 kHz pilot and the 433 MHz carrier are no longer be transmitted any more, which is recognised by the receiver. In that case after 15 seconds the receiver switches to standby.
   * Selection between the 7 channels around the 433 MHz.

2 Audio path
The basic audio path contains of plug 1409, input buffer IC7401A, a 15 kHz low pass filter L5401 (prevent high frequencies to the compander), a compander (IC7403 and IC7402B) and a buffer IC7404A.

3 Pilot generator
Although the transmitter transmits a mono signal, a pilot at 19 kHz pilot is used to enable the receiver to recognise whether the received signal is the wanted signal. This 19 kHz pilot is generated by an 38 kHz oscillator and a 2-divider around IC7404D/C.
Just before injection the pilot is added with the companded and buffered mono surround signal.

9.11.2 Compander

As the transmitter is an FM-transmitter, the amplitude of the audio and pilot signal is 'real time' converted into a FM-sweep. Large amplitudes are converted into a large FM-sweeps, small amplitudes into a small FM-sweeps. Small FM-sweeps have a bad signal to noise ratio and large FM-sweeps increase the required bandwidth. Therefore a so called 'compander' is used to limit the bandwidth and to increase the signal to noise ratio of the transmission. This compander attenuates large amplitudes (e.g. +10 dB to +5 dB), bypass middle amplitudes (0 dB to 0 dB) and boosts small amplitudes (e.g. -20 dB to -10 dB). On the receiver part this correction is corrected back by a so called 'expander'.
The basic compander configuration is given below. There is a variable gain cell (variable resistor inside NE572) in the feedback loop of an Op Amp (NJM). The resistance of the gain cell is controlled by the voltage across C2408 which is charged by the rectifier.

9.11.3 Pilot generation

The pilot oscillator is build around a 38 kHz tuning crystal 5403. Two inverters IC7404E and IC7404F - used as amplifiers - are used to make a buffered 38 kHz square wave signal.
The 38 kHz block is divided by 2 by the circuitry around the inverters IC7404D and IC7404C.

- On the moment the 38 kHz block becomes 'high', D6401 and TS7405 conduct. Via D6401 the input from IC7404D becomes 'high'. The output of IC7404D becomes 'low' and so the output of IC7404C becomes 'high' and keeps the input of IC7404D 'high'.
  As TS7405 conducts, C2438 is charged.
- On the moment the 38 kHz block becomes 'low', D6401 and TS7405 block. By now C2438 is discharged via R3449 as the input of IC7404C is still 'low'.
- On the moment the 38 kHz block becomes 'high' again, D6401 and TS7405 conduct. By now the input of IC7404D becomes 'low' as C2438 is still 'low' and TS7405 conduct. This 'low' on the input from IC7404D is long enough 'low' (via D6401 it wants to become 'high' again), to trigger the hold-circuitry IC7404D and IC7404C to a 'low' state.

The output is a sine wave due to the low pass filter R3450 and C2439. TS7406 is a buffer of the 18 kHz pilot generator.

9.11.4 Pilot and companded surround sound adding

The buffered and companded mono surround signal is fed to TS7410. This TS7410 has 3 functions:

- Adding the buffered and companded surround signal with the 19 kHz pilot.
- Buffer for the surround signal.
- Low-pass filter at 60 kHz via C2435.

Before injection into the modulator input there is the provision to align the maximum modulation (maximum FM sweep of 75 kHz) with potentiometer 3442.

9.12 Master and slave speaker box (Fig. 9.13)

9.12.1 General

The master and slave speaker box can be used wireless and wired. In case the system is used wired the cinch-plug on the master is used as input and the system automatically switches into the wired mode (by then as incoming signal from the TV the amplified surround signal from the rear speaker clickfit connector of the TV is used). Both wired and wireless make use of the amplifier in the master box. The slave box is a loudspeaker only which is driven by the master box. The following main circuitries are located inside the master box:

- Supply
- Receiver
- Amplifier

9.12.2 Supply

The supply consists of two conventional 50 Hz mains supplies.

- The standby supply is built up around mains transformer 5312. This standby supply starts immediately when the mains-switch TV-3 is switched on. By then via bridge rectifier D6312-6315 and stabiliser TS7275 the supply voltages V! and V2! are present.
- The main supply is built up around mains transformer 5313. This main supply is only active when the set is in normal operation and takes over the largest part of the energy delivery to stabiliser 7275 via D6260. In normal operation STBY_COM! is 'high', TS7273 blocks, TS7274 blocks, via R3316 TS7310 conducts and so relais 5310 is energized and the switch is closed.

Different situations:

- *Start up*
  At start up the system with mains switch TV-3, C2293 is charged but is even discharged faster via the 2 diodes D6278 and D6277. TS7272 blocks, TS7274 blocks, TS7310 conducts and so both supplies start up immediately.
- *Switch off*
  At switching off the system with mains switch TV-3, C2293 is not discharged any more via the 2 diodes D6278 and D6277. As a result C2293 is charged quickly and so immediately switches off the main supply. In this way a switch-off plop is prevented.
- *STBY_COM!*
  In case the STBY_COM! signal becomes 'low', the system must go into standby mode. In case STBY_COM! becomes 'low', TS7273 conduct, TS7274 conduct, TS7310 blocks and the main supply is switched off.
- If STBY_COM! is 'low' TS7265 will conduct and switch on the red LED. If STBY_COM is 'high', TS7265 blocks, TS7266 conducts and so the green LED is switched on.
  - ★ STBY_COM! 'low' → receiver in standby mode, main supply switched off, red LED
  - ★ STBY_COM! 'high' → receiver in normal operation, main supply switched on, green LED

9.12.3 Receiver

9.12.3.1 Block diagram

We can recognise 4 basic blocks in this diagram:

1. Frontend (1710):
   Here the incoming 433 MHz aerial signal is filtered, amplified and via a mixer converted to a fixed 10.7 MHz IF frequency. The frontend is housed in a separate shielding unit to minimise the local oscillator radiation. There is an antenna connected to the input of the frontend.
2. IF and decoder part (7710):
   Here the 10.7 MHz IF signal is filtered via 2 standard FM ceramic filters and fed to the IF FM-demodulator IC7710. In this IF FM-demodulator the mono surround signal is demodulated and the field strength and the presence of the pilot of the incoming 10.7 MHz signal is measured.
3. Audio path:
   The received audio signal is filtered and expanded in dynamic range, to correct the companding circuitry at the transmitter side. This circuit uses the NE572 hi-performance circuit with an extra opamp. Basically this circuit multiples the incoming dynamic range with a factor of 2 dB.
4. Microcomputer (7750):
   The μC reads the position of the 7-fold channel switch, controls the frontend via I²C and drives its mute pin.

9.12.3.2 IF demodulator

To make discrimination possible between the 7 channels that can be selected some selectivity has to made at the IF channel. Two standard 10.7 MHz ceramic filters with TS7707
in between are used for optimal behaviour towards S/N.
The IF-demodulator IC7710 (LA1805) has a main IF amplifier, and a FM and AM (not used) detector.
The IF-signal comes in at pin 1 and is boosted by a very high gain to a level where it is suitable for detection.
The detector needs a quadrature coil at pin 20.
The detected signal comes out at pin 17 and goes in again at pin 16. The stereodecoder is used for pilot detection only and is a classic system with a VCO (Voltage Controlled Oscillator) running at 152 kHz which can be adjusted by potentiometer 3721.
The AF outputs (pin 9 or/and 10) are filtered and amplified before they are presented to the expanding circuit. The filter 5730 is a double notch filter with filters out peaks at 19 and 38 kHz.

9.12.3.3 Expander circuit (IC7770)

The key IC is the NE572 which is used as an expander. Via this expander, the compander function in the transmitter side is corrected. This expander boost the high amplitudes (e.g. +5 dB to +10 dB), bypass middle amplitudes
(0 dB to 0 dB) and attenuates low amplitudes
(e.g. -10 dB to -20 dB).
The circuit is in fact a standard opamp (NJM) circuit where the input series resistor is formed by a gain cell. This gain cell is a variable resistor that is driven by a current that is obtained by rectifying the input current. Any variation of the cell impedance will change the gain of the main opamp NJM4560. Now the input of the gain cell and the rectifier are tied to the same level. When the input signal Vin drops by e.g. 6 dB, then the gain control current from the rectifier will also decrease with 6 dB (factor of 2).

Therefore the total change in Vout will be 12 dB, giving in fact a factor 2 (in dB) expansion. The detector circuit rectifies the input signal current. The V_{REF} for the opamp is extracted out of the NE572 IC via proper RC elements.

9.12.3.4 Microcomputer (IC7750)

The microcontroller is a MC68HC05 type with 1.2 kbit ROM and 14 I/O lines. The μC clock frequency is derived from a ceramic resonator of 4 MHz.
The internal clock is divided down to 500 kHz internally.
The reset circuitry around TS7755 creates a POR for the μC to assure that the μC only starts its program when the supply voltage is stable enough. The μC has the following functions:

- Read the setting of the 7 position slide switch continuously. In an internal look-up table the 7 required frequencies for the local oscillator are stored.
  The μC controls the local oscillator in the frontend 1710 to 1 of the 7 desired channels via the I^2C bus. The output towards the synthesiser chip in the front-end is in I^2C format, however there is no real handshaking as the synthesiser is the only device on the bus.
- In case the μC operates a channel switch, pin 11 is made 'high' for a moment. This to prevent plops when switching from one channel to another.
- In case the μC has detected that the receiver 1710 has received an incoming signal which is under the threshold level for more than 90 seconds, than pin 11 is made 'high' constantly.

9.12.3.5 MUTE signal

The MUTE signal on pin 5 of plug 1791 is 'high' in one of the following possibilities (OR-function):

- In case the 10.7 MHz field strength at the input of the IF-detector IC7710 is not strong enough. By then pin 8 of the IF-demodulator IC7710 and so - via D6710 - the MUTE signal becomes 'high'.
- In case the 19 kHz pilot-tone is not detected, pin 7 of the IF-detector IC7710 and so via D3710 the MUTE signal becomes 'high'. Even though the transmission is mono, this pilot tone is used and detected just to recognise that the received signal is the required signal.
- In case the μC operates a channel switch, pin 11 is made 'high' for a moment. This to prevent plops when switching from one channel to another.
- In case the μC has detected that the receiver 1710 has received an incoming signal which is under the threshold level for more than 90 seconds, than pin 11 is made 'high' constantly.

This MUTE signal is used for:

- Direct muting of the AUDIO signal at pin 2 of 1791 via mute circuitry TS7784 and TS7789. These transistors are connected inverse (collector and emitter are changed), but the functionality is the same. In case MUTE is high, the base-collector diode conducts and short the AUDIO signal via the emitter to the collector. In this way a better MUTE behaviour is obtained.
- Further this MUTE signal is fed to the circuitry which drives the STBY_COM! on the amplifier module.
  In case the MUTE signal is 'high' for more than 15 seconds, the STBY_COM! becomes 'low' and the receiver is switched to standby mode (see wireless mode).

9.12.4 Amplifier

This module can be used in two modes:

- Wireless mode
- Wired mode

9.12.4.1 Wireless mode

The amplified surround audio signal at the clickfits (diagram H2) can also be wired to the master box.
The input from the receiver is present at pin 2 of connector 1262 and fed via the emitter of TS7268 to the input of the amplifier. This signal can be connected to ground by TS7269 in case the STBY_COM! signal 'low' is. Pin 5 of 1262 is the mute pin.
When the MUTE is 'high', TS7270 conducts and pin 3 of comparator IC7262A becomes lower as the V_{REF} at pin 2 (4V6). As a result C2280 discharges via R3280. In wireless mode, the V_{REF} at pin 6 of IC7262B is 6V, and so it takes 15 seconds before pin 5 becomes lower as pin 6 of IC7262B. So in case the mute from the receiver is active for 15 seconds, by then the STBY_COM! will become 'low' and will switch the system to standby.

9.12.4.2 Wired mode

In case of wired use the switch in the cinch connector is open and so the supply voltage for the receiver at pin 3 of 1262 is not present any more. The audio signal - via pin 2 of plug 1260 - is fed to the AUDIO-IN! signal and to the low-level detector.
In wired use, the mute signal from the receiver-module should be disabled. If there is no voltage on pin 3 of 1262, pin 5 of 1262 will be forced high by R3305 and D6275 which means a mute state. This will force TS7270 in conduction as long as the wired mode is active. In this way D6276 is blocked and so the receiver-mute is disabled.
In the wired mode, a low-level detector is used, made by the circuitry around IC7260B and TS7260A. IC7260B and IC7206A are used as amplifier. The voltage divider R3320 and R3321 is used to limit the input signal to IC7260. C2269, C2295 and C2289 are used to block the DC-components. Via D6271 and D6272 only the positive pulses are fed though to pin 3 of comparator IC7262A. Only in case the audio level at the input of the low-level detector is lower as 3mV-RMS, pin 3 of comparator IC7262A becomes lower as the V_{REF} (4V6) at pin 2 and so the output at pin 1 IC7262A becomes 'low'.
As long as the input of the low-level detector is lower as 3mV-RMS, output pin 1 of IC7262A is 'low' and so C2280 is discharged via R3280. In case of a wired mode the threshold-level of comparator IC7262B is increased by a current through D6266 and R3277. As a result in wired mode the threshold level at pin 6 is decreased to 1V3. Therefor it takes 90 seconds before the discharged C2280 becomes lower than pin 6 of IC7262B. So only in case of 90 seconds no (or too low) sound, the STBY_COM! becomes 'low' and will switch the system to standby.

9.12.4.3 Amplifier

- IC7267 is the amplifier for both the master and the slave loudspeaker. It has an output power of 2x8W.
- To ensure a proper start up of the amplifier IC from standby to normal operation, pin 1 is used.
  Pin 1 filters the supply voltage at pin 12.
  * In normal operation STBY_COM! and so pin 6 of the IC is 'high' and so internally pin 12 is connected to pin 1.
  * In standby pin 6 is 'low' and so pin 12 is not connected any more to pin 1. During standby C2286 is precharged via the high STANDBY. This is done to realise a fast built up of the voltage at C2286 when the set is going from standby to normal operation in case of a bad charging of C2286 through IC7267.
- D6265 is used to charge C2282 to avoid plops at switching on.
- From normal operation to standby the following takes place in time:
  * Main supply of transformer L5513 is switched off inmediately, but C2314 is still charged.
  * Then C2290 is charged by the 'low' STBY_COM! signal and so - via the conducting TS7269 and TS7268 - the AUDIO-IN signal is muted.
  * Then C2284 is discharged by the 'low' STBY_COM! signal and so the standby pin 6 of amplifier IC7267 becomes 'low'. The amplifier is switched off after the AUDIO_IN is muted to avoid plops.
  * Then C2314 of the main supply is discharged and only the supply of L5312 is supplying energy to the stabiliser 7275.

DualScreen

9.13 Introduction

The wide picture version of the MD2.2 chassis can be provided with the DualScreen feature. In this there are two variants which can be distinguished:

- In the most basic version TXT or nexTView can be displayed next to the main picture. This is called 'text DualScreen'.
- In a higher specified sector it is possible, in addition to this, to display two video pictures simultaneously next to each other on the screen. This is called 'Video DualScreen'. When combined with text DualScreen this is designated as 'full DualScreen'.

Text DualScreen (video/TXT or video/nexTView)

The picture is divided into two, in a horizontal ratio of 60/40. These two parts are filled as follows:

- The video information is compressed horizontally and pushed left to the left-hand 60% of the picture by means of the PANIC on the Feature Box.
- The TXT or nexTView information is compressed horizontally and pushed right to the right-hand 40% of the picture by means of a circuit on the TXT+control module.

The total picture is further compressed vertically by means of the DDP.

Video DualScreen (video/video with sound of the second video picture on the headphones plug)

Two different video pictures are displayed next to each other in a horizontal ratio of 50/50, whereby the sound of the second video channel is fed to the headphone plug. This is achieved using the so-called 'video DualScreen' and 'YUV interface' modules and modified Dolby Audio Module:

- The 1fH YUV main signal is branched off immediately after TDA9143 on the SSP via the YUV interface panel and is fed to the Video DualScreen module.
- The 1fH YUV sub-signal from the second video picture is created on the Video DualScreen module by means of a 2nd tuner, an MF-demodulator and a TDA 9143.
- The YUV main and sub-signals are placed next to each other in the PIPO (Picture In Picture Out). The YUV output signal (YUV-DW) is still always on the base of 1fH and is fed back to the YUV interface. There is a YUV switch on the YUV interface:
  * If the Video DualScreen feature is not activated, the YUV main signal from TDA9143 on the SSP is immediately looped through to the Feature Box.
  * If the Video DualScreen feature is activated, the YUV-DW signal is fed to the Feature Box.

If the Video DualScreen feature is activated, the sound of the second video channel is fed to the headphones plug via a modified Dolby Audio Module.

9.14 Text DualScreen

9.14.1 Horizontal compression of the TXT/nexTView information (Fig. 9.14)

Principle

- SK1 and SK2 are components of the Blending circuit (see chapter Video Processing).
- The TXT information is compressed by the RGB info to be written into a memory and then read out on a double frequency.
- In order to be able to display the TXT information in the 40% screen, all level 2.5 features, including the side panel feature, are switched off by the software. The maximum number of characters which can be displayed per line is reduced from 56 to 40. Since nexTView also makes use of these possibilities it also has the result that the layout of this is modified in nexTView DualScreen mode.
- In order to set the analogue RGB signals at the correct digital level for the memory IC7462 (after all, this IC can only process digital information), an additional buffer has to be fitted between IC7462 and the TXT-IC, IC7400, namely IC7461. Because IC 7461 also inverts the signal, then after reading out from IC7462 an inverter IC7463 is used in order to 'straighten' the signal again.
- Because IC7461 discriminates the RGB (and FBL) level to high or low (no longer any interim steps) TXT level 2.5 colours (32 colours) is automatically returned to TXT level 1.5 colours (8 colours) if text DualScreen is active.
- With the DWE (Double Window Enable) switch line, originating from the operating mP, a selection is made between a complete TXT/nexTView picture or a DualScreen. If DWE is low, the text DualScreen is displayed.

Ciruit description

Remark:
Due to the software suppression of level 2.5 features in DualScreen mode, then not only will the side panel feature be switched off but also the background colours, DRCS, etc.

Writing to and reading out of the memory

- The TMS4C1050B (IC7462) is a 4 bit organized memory. This memory is addressed via 2 independently operating reading and writing address counters. In addition to this the IC has a separate data write bus A and a separate data read bus B.
- The D0, D1, D2, D3 inputs are used to write the Blanking and RGB signals into the memory. The following signals are used to control the writing section:
  * **W**rite enable (W) releases the write address counter and gives permission for data to be written into the memory.
  * **R**e**S**e**T** **W**rite (RSTW) provides a reset for the write address counter.
  * **S**erial **W**rite **C**loc**K** (SWCK) is a clock signal which determines the writing speed of the memory.
- The Q0, Q1, Q2, Q3 outputs are used to read out the Blanking and RGB signals from the memory.
  The following signals are used to drive the reading section:
  * **R**ead enable (R) releases the read address counter and gives permission for data to be read out of the memory.
  * **R**e**S**e**T** **R**ead (RSTR) provides a reset for the read address counter.
  * **S**erial **R**ead **C**loc**K** (SRCK) is a clock signal which determines the reading speed of the memory.

In text DualScreen the frequency of the read clock is double that of the write clock.

Creating the clock signals in order to be able to read and write in the Field Memory

In order to provide the memory IC, IC7462, with the required clock pulses, the following circuits are made:
- The TXT-IC gives pin 39 a TCASIN with a frequency of 12 MHz with its harmonic. A band pass filter, with an adjustable coil L5465, only allows the 2nd harmonic to pass. This 24 MHz is used directly as a read clock (SRCK). In order to obtain a synchronous running writing clock (SWCK) which is exactly half the speed of the read clock, the signal is driven through a 2 divider IC7465/A.
- The TXT/IC delivers on pin 3 a line frequency pulse with a duty-cycle of exactly 50% (signal PL). This pulse is used as the clock input for the 2nd flip flop IC7465/B. The vertical flyback pulse (VFB) arrives on the D input. A reset read (RSTR) and a reset write (RSTW) are therefore generated at raster frequency. Since there is a time difference between the two trigger points (rising slope) of these reset signals, the 12 MHz clock is held up to the START moment. In this way the writing and reading are exactly synchronized.
- At the START moment the RSTR is high. As a result of this the 12 MHz write clock is released and the writing into the memory begins. This is exactly at the rising PL slope. The writing is now no longer interrupted until a further frame flyback. A full raster is therefore written into the memory.
- The reading of the memory is stopped just at the moment of START (Read enable is low). Only in the second half of the PL pulse (this is a half line time later) does the Read Enable become high. As a result of this the read address counter is released and the reading out of the memory starts. Since the read address counter is running at 24 MHz clock this reading out runs twice as fast as the writing. Another half a line time later the Read Enable again becomes low and reading out stops again.
  This cycle repeats itself for each line.
  * During the first half of the line the PL is high, the read enable (R) is therefore low; nothing is therefore read out.
  * During the second half of the line the PL is low and the memory is read out at double speed (24 MHz clock)

9.14.2 Horizontal compression of the video information

In addition to the compression of the TXT/nexTView section, the video section of the picture should also be compressed. For text DualScreen this horizontal compression is achieved by the PANIC IC in the FBX. Via a software command the picture is compressed in the PANIC and pushed horizontally to the left.

9.14.3 Horizontal centring of text DualScreen

In order to arrange the video and TXT/nexTView information neatly at the correct distance beside each other, initially the TXT/nexTView half on the right is set against the side of the picture by the DDP. After this, by means of the software centring of the FBX, the video half is set to the correct horizontal distance with regard to the TXT/nexTView information.

9.14.4 Vertical compression of the text DualScreen picture

The total picture for text DualScreen is compressed vertically with the aid of the DDP (vertical deflection is adjusted) in order to again obtain the correct height/width ratio of the video picture. As a result of this black bars are created on the top and bottom of the picture.

9.15 Video DualScreen

9.15.1 Introduction

The video DualScreen picture consists of 2 sections of the same size:
- the left-hand section is the main picture originating from the main tuner or from RGB, CVBS or SVHS signals from external sources.
- the right-hand section is the sub-image originating from the 2nd tuner or from CVBS or SVHS signals (no RGB signals) from external sources. The video decoding for the sub-image takes place on the Video DualScreen module and makes no use of the COMB filter. The result is that the picture quality of the sub-image is generally less than that of the main picture.

9.15.2 Block diagram

The following blocks can be distinguished on the Video DualScreen:

- PLL tuner E9F1 is a UV1216D which is driven via I^2C.
- A TDA9815 is used for MF demodulation.
  The PCF8574AT controller IC9N is used in order to set the switching signals from the MF demodulator into the correct mode.
- Via a source selector IC9L a selection is made between TUN_CVBS (from the Video DualScreen tuner) or CVBS PIP (from the TEA6415 source selector on the SSP). At the same time this IC9L can be used to select between CVBS-PIP or YC-PIP.
- The Y/CVBS-PIP or CVBS TUNER signal and the C-PIP signal are fed to the TDA9143 IC9J on the Video DualScreen module. Together with the delay line IC9K the CVBS or SVHS signal is converted here to the SUB-YUV signals together with the sync signals SPHsync and SPVsync. The RGB-TXT inputs of this TDA9143 are not used here.
- The sub-YUV signals (SY, SU, SV) together with their sync signals SPVsync and SPHsync and the Main-YUV signals (MU, MY, MV) with their sync signals HA = SC_1fH = DPVsync are placed next to each other in the PIPO (Picture In Picture Out) IC9A SAB9077. The RAM IC9E is used as the memory.
- The output of the SAB9077 DW-YUV signals (DY, DU, DV) are fed directly to the output of the Video DualScreen panel to the YUV interface (in the MD2.2 the function of the switching IC IC9M is on the YUV interface, therefore IC9M and the switching signals DFB1 and DFB2 are not used). Via the switching signal FBLK the YUV interface can be set to the bypass mode (FBLK 'low') or to the Video DualScreen mode (FBLK 'high').
- If the Video DualScreen feature is not active, part of the +5V supply voltages (+5VSW) is switched off via Q9N1 and switching signal VDS STANDBY (VDS STANDBY becomes 'low' (standby mode) 60 seconds after the VDS feature is switched off. As a result of this the load of the +5V supply voltage reduces if the Video DualScreen feature is not used. Because the PIPO is also switched off, then via IC9P and VDS TSNADBY = 'low', the HA and VA sync signals are not looped through to the HA' and VA' sync signals which go to the PIPO. This prevents the non-active PIPO loading the HA and VA signals.
- Because the TXT/nexTView DualScreen are created by a totally different signal path in the MD2.2, connector J9A5, J9A6, the buffers around Q9P1, Q9R1 and Q9S1 and the section of pin 12, 13, 14 of IC9L are not used.

9.15.3 Tuner and MF section

The tuner is an I^2C controlled PLL tuner with built-in splitter. The antenna input goes to the Video DualScreen module and is split there into the main and Video DualScreen tuner. The D_TUN pin 8 is the supply for the splitter section. The ADDRESS pin 15 is used to give this tuner a different address on the I^2C bus of the main tuner.

The MF section can handle all of the systems throughout the world and is constructed around the MF demodulator IC9R, the TDA9815 (also used in GR2.4). This is, with regard to pinning, the same as the TDA9811 of the MD2 MF module, however, in the TDA9815 an FM demodulator is built in. In order to select the correct demodulation system and the correct filtering, the following switching signals are used. These switching signals originate from the PCF8574AT IC9N.

System	BG/LL'IMDK	L'	I	POS/NEG	M
BG	1	0	0	1	0
L	0	0	0	0	0
L'	0	1	0	0	0
I	0	1	1	1	0
M	0	0	0	1	1
DK	0	0	0	1	0

The video path

- *BG via SAW filter FL90*
  BG/LL'IDKM is 'high', D9G0 conducts, D9G1 reverses. As a result of this IF2 becomes short-circuited and IF1 is fed to the Video IF inputs pin 1 and 2 of the TDA9815 via the BG SAW filter FL90.
- *LL'IDK via SAW filter FL91*
  BG/LL'IDKM is 'low', D9G0 reverses, D9G1 conducts. As a result of this IF1 becomes short-circuited. Because M-TRAP is 'low', D6G2 reverses and D9G3 conducts as a result of which the IF2 is fed to the LL'IDK SAW filter FL91.
  At the same time D9G5 conducts and D9G4 reverses because M-TRAP is 'low'. As a result of this pin 4 and 5 of FL92 (M SAW filter) become short-circuited and pins 5 and 4 of FL91 (LL'IDK SAW filter) are not short-circuited. Therefore, pins 5 and 4 of FL91 are looped through to pins 4 and 5 of TDA9815 respectively.
  The circuit around L9F2 filters out the sound at 40.4 MHz from the adjacent channel.
- *M via SAW filter FL92*
  BG/LL'IDKM is 'low', D9G0 reverses, D9G1 conducts. As a result of this IF1 becomes short-circuited. Because M-TRAP is 'high', D6G2 conducts and D9G3 reverses as a result of which the IF2 is fed to the M SAW filter FL92.
  At the same time D9G5 reverses and D9G4 conducts because M-TRAP is 'high'. As a result of this pins 4 and 5 of FL91 (LL'IDK SAW filter) are short-circuited and pins 5 and 4 of FL92 (M SAW filter) are not short-circuited. Therefore, pin 4 and 5 of FL92 are looped through to pins 4 and 5 respectively of the TDA9815.
- Pin 30 selects the MF inputs: 'high' for the BG VIF inputs pin 1-2 and 'low' for the LL'IDKM VIF inputs pin 4-5.

- In order to filter sound from the Video IF (VIF), the series connected band reversing filters X9T4, X9T5 and X9T6 are used. X9T4 is only connected in series in the M mode (M-TRAP 'high' therefore Q9F5 reverses and Q9F6 conducts). Pin 21 is the output, pin 22 the input. Finally, the buffered TUN-CVBS signal is present on pin 10.
- AFC oscillator between pins 23 and 24 which is adjusted to 77.8 MHz (2 x 38.9 MHz). The adjustment takes place via pin 23 of the AFC detector. The AFC loop of the Video DualScreen demodulator is not used. The AFC loop of the main demodulator on the IF module of the set itself is used to correct any drift of the transmitter for both the main tuner and for the Video DualScreen.
- Pin 9 is 'high' for BGIDKM (negative modulation) and 'low' for LL' (positive modulation).
- Pin 11 is 'low' in the L' mode (L' 'high') or in the M mode (M-TRAP 'high') via Q9F1. A low pin 11 is interpreted in the positive modulation mode (pin 9 'low') in order to de-tune the 38.9 MHz to 32.4 MHz. In the negative modulation mode (pin 9 'high') a low pin 11 is interpreted in order to select sound input pin 18 (M audio input) instead of the sound input pin 17 (BGLL'IDK audio input).
- Pin 7 is switchable for the PLL loop filter. For BGIDKM, R9H9 is short-circuited via Q9F2 as a result of which the time constant is changed.
- Pin 6 is used in order to adjust the AGC takeover point via R9H5.

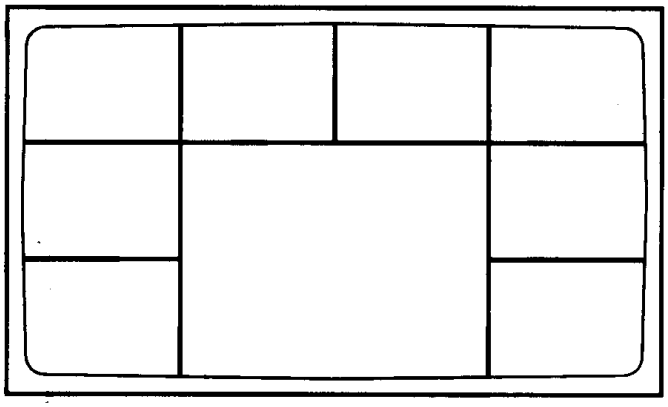
The sound path

The TDA9815 delivers an FM mono or AM mono. Via L9F8 the sound path is disconnected from the picture path.

- *BG via SAW filter FL93*
  L' is 'low', D9G8 conducts, D9G9 reverses, pin 6 of the L9F8 is short-circuited via C9T5. Therefore, the MF signal from the tuner is fed via pin 4 of L9F8 to pin 1 of FL93 (BG SAW filter) and pin 2 of FL94 (LIDK SAW filter). Because BG/LL'IMDK is 'high', D9G6 conducts and D9G7 reverses. As a result of this pins 4 and 5 of FL94 (LIDK SAW filter) are short-circuited and pins 5 and 4 of FL93 (BG SAW filter) are not short-circuited. Pins 5 and 4 of FL93 (BG SAW filter) are looped through to pins 31 and 32 of TDA9815 respectively.
- *LIDK via pin 2 SAW filter FL94*
  L' is 'low', D9G8 conducts, D9G9 reverses, pin 6 of the L9F8 is short-circuited via C9T5. Therefore, the MF signal from the tuner is fed via pin 4 of L9F8 to pin 1 of FL93 (BG SAW filter) and pin 2 of FL94 (LIDK SAW filter). Because BG/LL'IMDK is 'low', D9G6 reverses and D9G7 conducts. As a result of this pins 5 and 4 of FL93 (BG SAW filter) are short-circuited and pins 5 and 4 of FL94 (LIDK SAW filter) are not short-circuited. Pins 5 and 4 of FL94 (LIDK SAW filter) are looped through to pins 32 and 31 of TDA9815 respectively.
- *L' via pin 1 SAW filter FL94*
  L' is 'high', D9G8 reverses, D9G9 conducts, pin 4 of the L9FB is short-circuited via C9T5. Therefore, the MF signal from the tuner is enabled via pin 6 of L9F8 to pin 1 input of FL94 (L' SAW filter). Because BG/LL'IMDK is 'low', pins 4 and 5 of FL94 are looped through to pins 31 and 32 of TDA9815 respectively.
- *M sound inter-carrier*
  In M mode the sound inter-carrier is processed, therefore the sound is extracted from the VIF information. Because the sound path is not used it is disabled by Q9F7.
- In order to filter the sound signal (SIF) from the picture the band reverse filters X9T0, X9T1, X9T2 and X9T3 are used. Pin 20 is the output, pin 18 the input for M sound and pin 17 the input for BGLL'IDK sound. Filter X9T1 (6.0 MHz) is switched off in the BG mode in order to prevent any NICAM BG carrier (5.85 MHz) from passing and filter X9T2 (6.5 MHz) is switched off in the I mode in order to prevent any NICAM I carrier (6.552 MHz) from passing.
- Pin 12 is the DW-MONO output. Via Q921 the de-emphasis for BGIDKM can be modified and additionally modified for M via Q922.

9.15.4 MultiScreen with the PIPO

In a set with the Video DualScreen module, Multi PIP is no longer created but MultiScreen is created with the aid of the PIPO SAB9077. In the MD2.2 the following configuration is selected:



76532013_010.AI
060397

For this the large picture is the main picture from the main tuner. The 8 small pictures are created by the Video DualScreen tuner. At the same time a scan or photofinish can be created with the 8 small pictures, for which the picture at the bottom right is the live picture.

Blockschaltbild nicht Top-Dolby-Version /

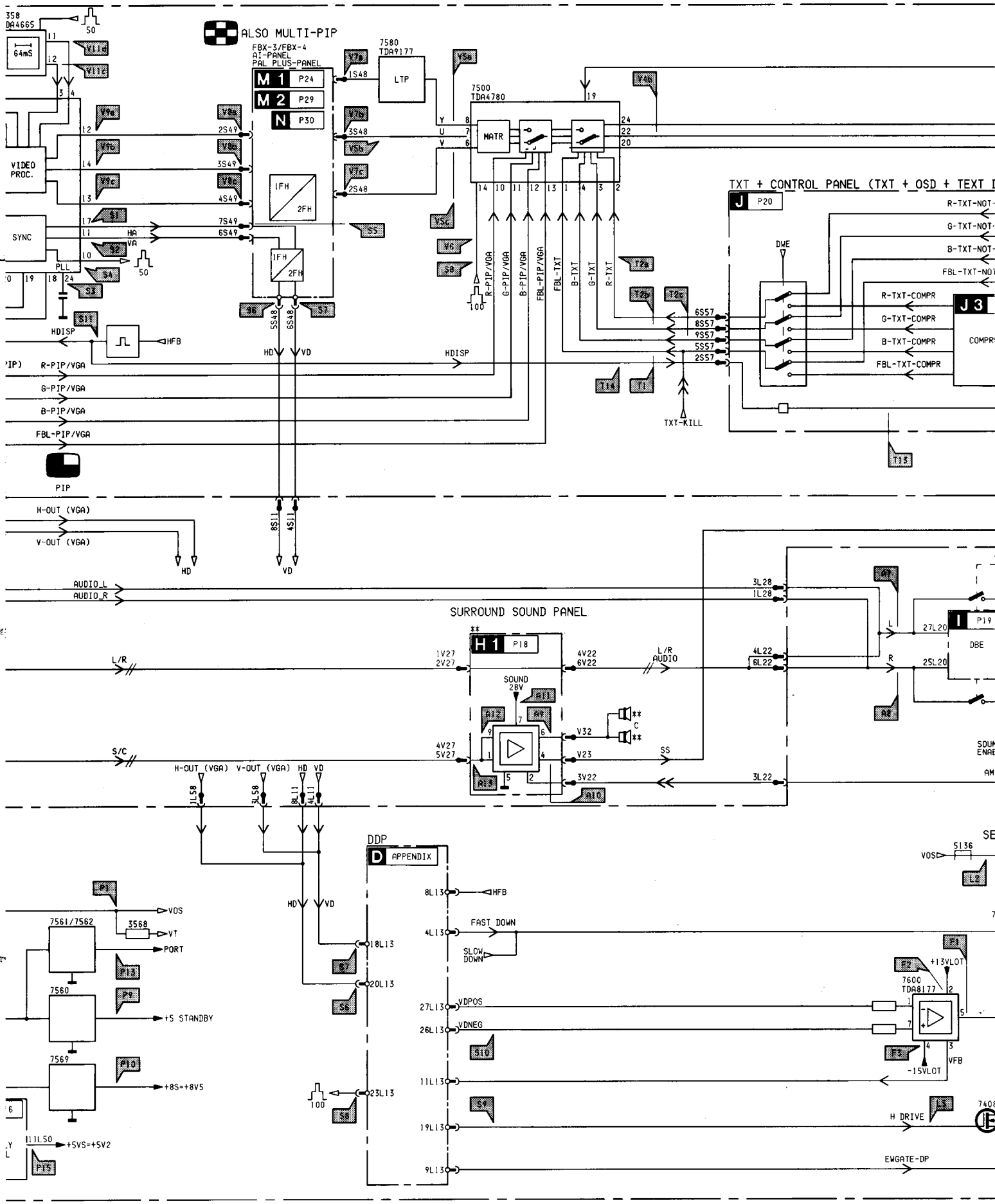
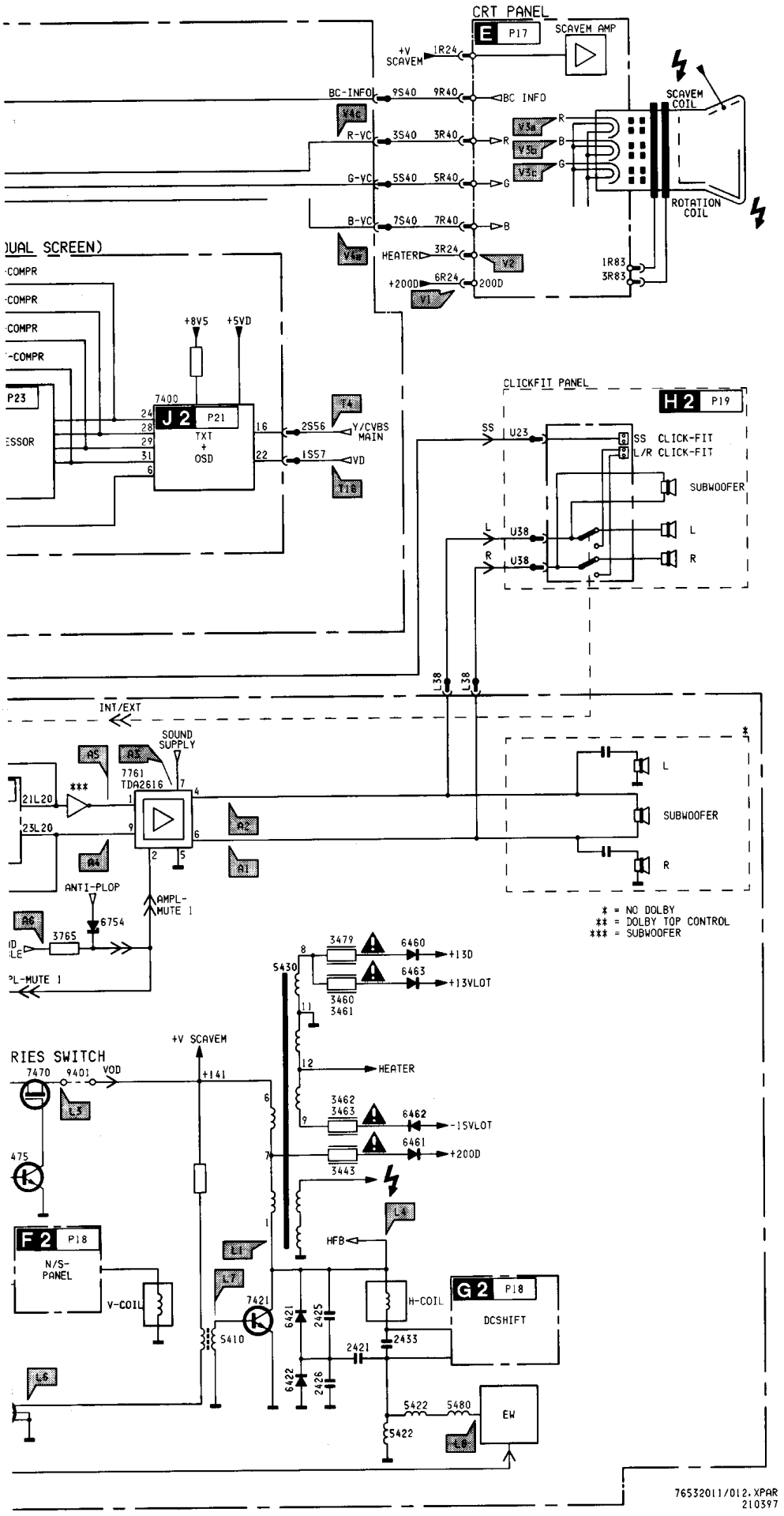
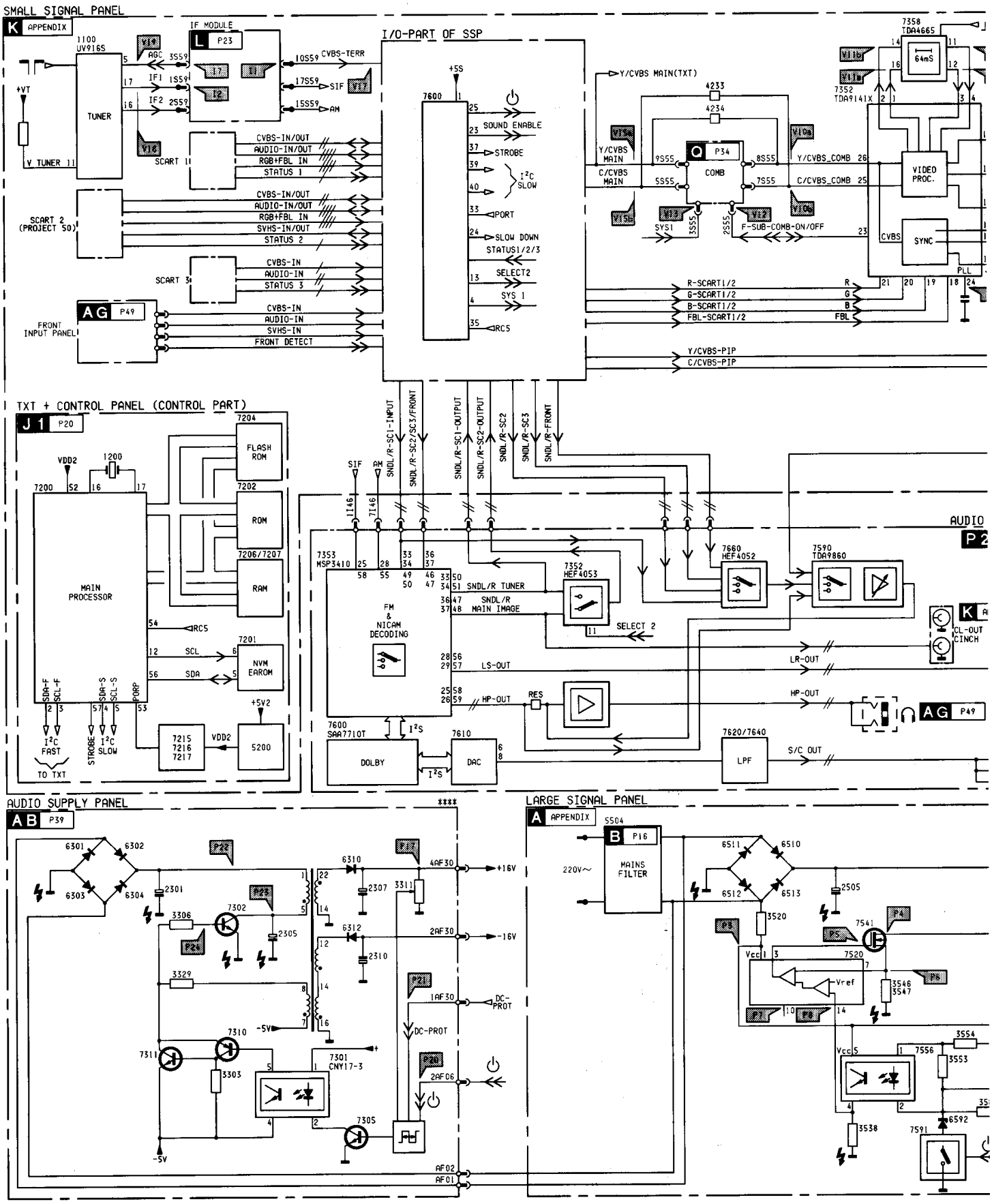


Diagramme synoptique version non Top-Dolby



Block diagram Top-Dolby version (front control styling) /



Blockschaltbild der Top-Dolby-Version /

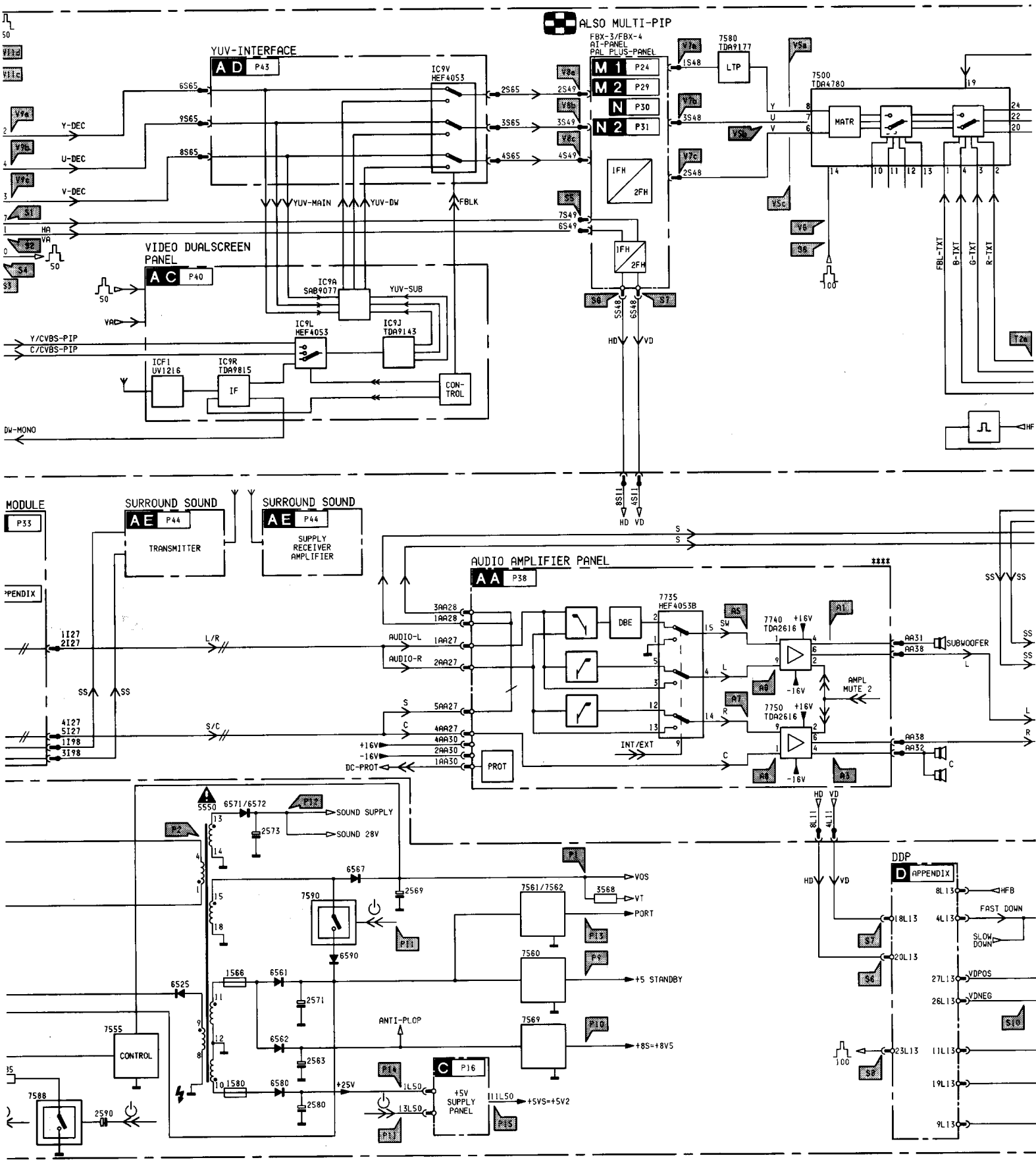
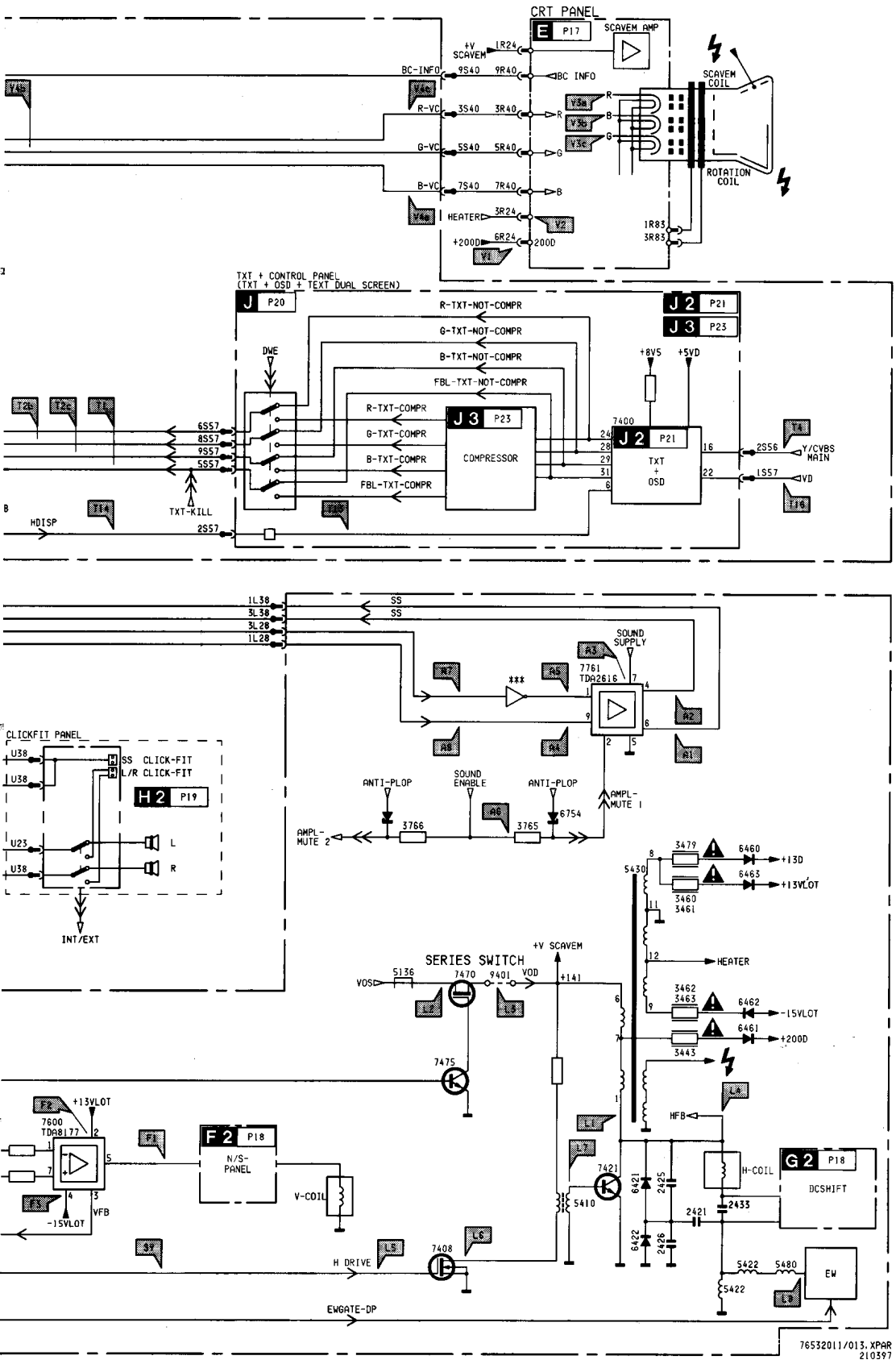


Diagramme synoptique de la version Top-Dolby



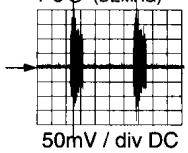
002	K6	7480	D4	3523	I9	5567	F6	9427	I5	9618	D3	2596	D7
003	D3	7507	M9	3525	I9	5572	F7	9428	H3	9619	A4	2601	B1
004	B8	7520	I9	3526	I9	5573	D10	9429	H4	9620	A2	2609	C5
005	F7	7541	J7	3527	I9	5617	E2	9431	H2	9621	C2	2612	D1
1503	N7	7556	H10	3529	K8	5701	B8	9432	I2	9622	D2	2613	D1
2400	G4	7560	E9	3530	J10	6409	N3	9433	H3	9624	A4	2614	D2
2418	L5	7569	B9	3531	K9	6410	N4	9435	G2	9749	A9	2615	C3
2419	K5	7590	E7	3532	L10	6411	N5	9436	I2	9750	B6	2616	D1
2420	K5	7600	D1	3533	K10	6425	I3	9440	K4	9751	A8	2617	E1
2421	G3	7761	B6	3534	K10	6426	I3	9441	K4	9752	A8	2618	D2
2422	F3	L01	N8	3535	I10	6441	L2	9442	C2	9753	B10	2620	E2
2425	J4	L02	M10	3536	I10	6451	B4	9443	C3	9754	A9	2630	B5
2426	H5	L04	M7	3537	I10	6452	C3	9444	F1	9755	A8	2750	C8
2428	I4	L06	C10	3538	H10	6453	M3	9445	H3	9756	A8	2751	A10
2432	H3	L07	D10	3539	I10	6454	M3	9446	H3	9758	N7	2752	A10
2433	H3	L10	E10	3541	J7	6460	J1	9447	E3	9759	A9	2753	B6
2434	H5	L11	A5	3546	K7	6462	G2	9450	M3	9760	B8	2754	C7
2442	L2	L13	A4	3547	K7	6463	G2	9451	I2	9761	B10	2756	A6
2450	M2	L15	A3	3548	I9	6465	G4	9453	J1	9762	B8	2761	B6
2452	M2	L17	L4	3549	H9	6466	M2	9456	H2	9767	N7	2762	B7
2453	M2	L20	C8	3550	H9	6471	G5	9458	L1	9781	B6	2763	B7
2466	F2	L22	A9	3551	H9	6479	D4	9460	I2	9782	D8	2776	A6
2478	E5	L24	M1	3552	K10	6480	C4	9461	H2	9786	B10	2778	A7
2505	L8	L25	C1	3553	F9	6481	C4	9462	H1	1440	E2	2787	B7
2506	M10	L28	B10	3554	E9	6482	D4	9463	F2	1566	G8	2788	A6
2509	M9	L38	A8	3555	F10	6483	E3	9465	B4	1572	G8	3401	F4
2540	K7	L39	A8	3556	G10	6506	M9	9466	C4	1580	G8	3402	F4
2542	I7	L50	E8	3557	G10	6507	J8	9470	G5	2401	F4	3443	L1
2543	J7	L58	A1	3558	G10	6508	M9	9471	F6	2402	N3	3460	H2
2544	J7	L91	H3	3560	F9	6509	L9	9472	B5	2409	A4	3461	G2
2550	H9	L93	H4	3561	F9	6510	M7	9473	B5	2410	M3	3462	H1
2561	D8	2504	L7	3562	G6	6511	M6	9475	B5	2411	N4	3463	H1
2563	F7	2531	J10	3563	E9	6512	M8	9476	F4	2412	N4	3479	J2
2566	D8	3407	N3	3564	C7	6513	M8	9477	H4	2413	N4	3502	I8
2567	G6	3409	N2	3565	E9	6514	L9	9478	E4	2417	M5	3513	M9
2568	G6	3411	M4	3566	E9	6515	K9	9479	E5	2424	I3	3524	K8
2569	H6	3412	M4	3568	E10	6516	K9	9481	E3	2431	I4	3543	I8
2573	E6	3413	N3	3569	E9	6518	I9	9482	D4	2435	H3	3559	F10
2580	F8	3414	B4	3570	G7	6524	K9	9508	J8	2440	L2	3609	C5
2755	C7	3416	N2	3571	D9	6525	J8	9509	F10	2448	C4	3617	F1
2765	A7	3417	M4	3572	F9	6540	K7	9510	D9	2457	C4	3622	B2
2766	B8	3418	M4	3579	J10	6541	K7	9520	I10	2460	J1	3752	A6
2767	A7	3419	J5	3582	D9	6542	I7	9522	K8	2461	I1	3753	C6
2768	B8	3425	H5	3583	D7	6545	J6	9523	K8	2462	F2	7408	N4
3400	G3	3426	H4	3584	F9	6548	I8	9525	I9	2463	G2	7409	N3
3408	N5	3430	J4	3585	F9	6550	G10	9526	I9	2465	G1	7512	L8
3410	N5	3431	J4	3586	F9	6560	F8	9530	J10	2467	E5	7513	L9
3415	N1	3434	I3	3587	F9	6561	F8	9536	H9	2468	G5	7514	L9
3423	I5	3435	I3	3588	E9	6563	D8	9537	H10	2480	E4	7515	L10
3453	M3	3448	B4	3589	E7	6564	A6	9543	F7	2481	C4	7555	G10
3478	L1	3449	C3	3592	G9	6566	K7	9544	H9	2482	C5	7561	E9
3503	M6	3450	M1	3593	E6	6569	C10	9545	I7	2503	J8	7562	E10
3505	M6	3451	M2	3594	D7	6576	D8	9551	G8	2507	J8	7588	E10
3506	N9	3452	M2	3595	D7	6577	E7	9552	H9	2508	L9	7589	F9
3507	N10	3457	B4	3596	D9	6581	F8	9557	F6	2511	M7	7591	G9
3528	M9	3458	C4	3597	G9	6590	E6	9560	D10	2512	M8	7592	D6
3544	I7	3459	M3	3598	F9	6591	D7	9561	F6	2513	L9	7770	C8
3545	K6	3465	B5	3599	E6	6592	G9	9562	E7	2514	K9		
3567	F6	3466	C5	3601	C1	6614	E2	9563	D10	2521	J9		
3573	D6	3467	D5	3602	C1	6617	C2	9564	G6	2522	J9		
3574	D6	3468	G5	3603	C1	6618	C2	9565	D9	2524	I9		
3575	C6	3469	L1	3610	C2	6620	E2	9569	C10	2525	I8		
3590	E6	3470	F5	3611	C1	6753	B9	9571	F6	2526	H8		
5400	G5	3471	F5	3612	B2	6754	C9	9572	F7	2527	I8		
5401	G4	3472	D5	3613	B3	6755	C8	9573	D6	2528	J9		
5402	H6	3473	D5	3614	B3	6756	C9	9574	D6	2533	K10		
5410	M4	3474	B5	3618	B1	6757	B9	9575	D10	2534	J10		
5411	M5	3475	E5	3619	B1	6770	C9	9576	D9	2535	I10		
5421	I4	3476	F5	3620	F1	9400	F3	9577	D10	2538	H10		
5422	E3	3477	D5	3750	C6	9401	G4	9578	D9	2541	K8		
5423	I5	3480	C4	3751	C6	9402	F1	9579	E7	2545	J6		
5424	F3	3481	C4	3755	A7	9403	C2	9581	J9	2548	H9		
5430	K3	3482	E2	3760	B6	9405	F2	9585	F9	2554	G10		
5460	I2	3483	C3	3761	B6	9406	C2	9592	G8	2555	G10		
5461	H2	3484	C3	3762	B7	9407	F2	9597	D9	2557	G10		
5462	H1	3485	D4	3763	C7	9408	M5	9600	E1	2559	C10		
5480	D3	3486	D4	3764	B7	9409	J2	9601	B3	2560	F8		
5507	M9	3487	B4	3765	C8	9410	N5	9602	B3	2562	H6		
5550	H7	3488	C5	3766	B9	9411	H4	9603	A5	2564	E8		
5750	C6	3489	E3	3770	C8	9412	D5	9604	B2	2565	C10		
5751	C6	3508	L9	3771	C8	9413	A2	9605	B2	2570	G7		
6419	L5	3509	L10	3772	C8	9414	A2	9606	B4	2571	E9		
6421	I5	3510	J8	5418	L5	9415	D4	9607	B4	2572	F7		
6422	H5	3512	K9	5419	L5	9417	M5	9608	B5	2574	E9		
6562	F8	3514	L10	5425	H5	9419	L5	9609	C2	2575	D6		
6567	G6	3515	K10	5426	L5	9420	I4	9610	A2	2581	F9		
6571	F7	3516	K10	5525	I8	9421	K4	9611	E4	2584	F10		
6572	F7	3517	L9	5542	J7	9422	H6	9612	D1	2590	F10		
6573	E6	3518	I9	5543	F7	9423	H5	9613	C1	2591	F10		
7421	L5	3519	K10	5544	I7	9424	H4	9615	A3	2592	D6		
7470	F5	3521	J9	5545	I6	9425	H5	9616	B3	2593	F6		
7475	E4	3522	K8	5561	D8	9426	L5	9617	A3	2594	F7		

POWER SUPPLY

P1 ⏀ (VOS)
140V DC

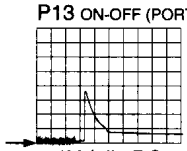
P1 ⏻ (VOS)
0V DC

P6 ⏻ (DEMAG)



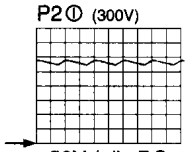
50mV / div DC
0.1s / div

P13 ON-OFF (PORT)



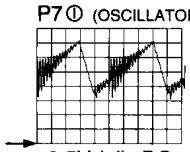
1V / div DC
1s / div

P2 ⏀ (300V)



50V / div DC
5ms / div

P7 ⏀ (OSCILLATOR)



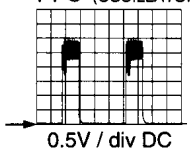
0.5V / div DC
5µs / div

P14 ⏀ (+25V)
27V5 DC

P2 ⏻
300V DC

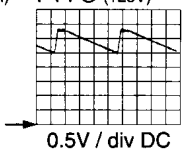
P3 ⏀ (Vcc IC7520)
14V DC

P7 ⏻ (OSCILLATOR)



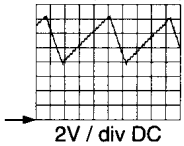
0.5V / div DC
0.1s / div

P14 ⏻ (+25V)



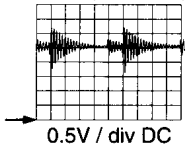
0.5V / div DC
20ms / div

P3 ⏻ (Vcc IC7520)



2V / div DC
20ms / div

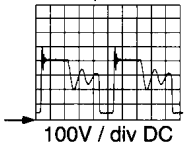
P8 ⏀ (FEEDBACK)



0.5V / div DC
5µs / div

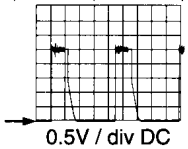
P15 ⏀ (+5S)
25V DC

P4 ⏀ (DRAIN TS7541)



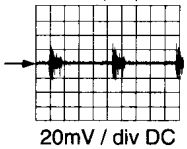
100V / div DC
5µs / div

P8 ⏻ (FEEDBACK)



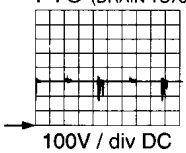
0.5V / div DC
20ms / div

P15 ⏻ (+5S)



20mV / div DC
20ms / div

P4 ⏻ (DRAIN TS7541)



100V / div DC
0.1s / div

P9 ⏀ (+5V STANDBY)
4V9 DC

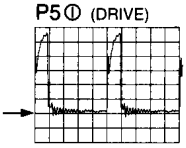
P9 ⏻ (+5V STANDBY)
4V9 DC

P10 ⏀ (+8S)
8V6 DC

P10 ⏻ (+8S)
0V DC

HORIZONTAL (LINE)

P5 ⏀ (DRIVE)



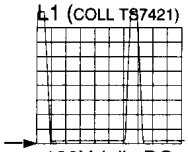
2V / div DC
5µs / div

P11 ⏀ (STANDBY)
3V9 DC

P11 ⏻ (STANDBY)
0V1 DC

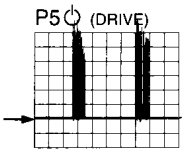
P12 ⏀ (SOUND-SUP.)
29V5 DC

L1 (COLL TS7421)



100V / div DC
5µs / div

P5 ⏻ (DRIVE)



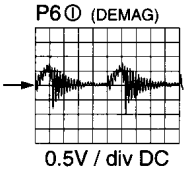
0.5V / div DC
0.1s / div

P12 ⏻ (SOUND-SUP.)
3V DC

L2
(TS7470 series switch)
140V9 DC

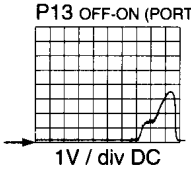
L3
(TS7470 series switch)
140V4 DC

P6 ⏀ (DEMAG)



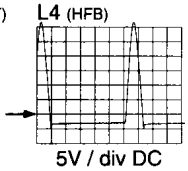
0.5V / div DC
5µs / div

P13 OFF-ON (PORT)



1V / div DC
20ms / div

L4 (HFB)



5V / div DC
5µs / div

Overview oscillograms / Übersicht der Oszillogramme /

L5 (HDRISE)
1V / div DC
5 µs / div

SYNCHRONISATION

S9 (HDRIVE)
1V / div DC
5 µs / div

V4b (RGB IC7500)
1V / div DC
10µs / div

V8a (YUV DEC)
0.2V / div AC
10µs / div

V11b -(B-Y)
0.2V / div AC
20µs / div

V18 (IF1)
50mV / div DC
50µs / div

A5 (L
(volume
50m
0.5

L6
50V / div DC
5µs / div

S1 (HA)
1V / div DC
10µs / div

S10 (VDNEG)
0.2V / div DC
5ms / div

V4c (RGB IC7500)
1V / div DC
10µs / div

V8b (YUV DEC)
0.2V / div AC
10µs / div

V11c -(U)
0.2V / div AC
20µs / div

V19 (AGC)
1V9 DC

IF

A6 (S
MUT
MUT
A11 (
27V

L7 (BASE TS7421)
2V / div DC
5µs / div

S2 (VA)
1V / div DC
5µs / div

S11 (HDISP)
1V / div DC
10µs / div

V5a (YUV IC7500)
0.2V / div AC
10µs / div

V8c (YUV DEC)
0.2V / div AC
10µs / div

V11d -(V)
0.2V / div AC
20µs / div

I1 (CVBS_TERR)
0.5V / div DC
10µs / div

A7 (A
(volume
50m
0.5

L8 (EWD)
10V / div DC
2ms / div

S3 (PLL)
50mV / div AC
10µs / div

VIDEO

V1 (+200D)
200V DC

V5b (YUV IC7500)
0.2V / div AC
10µs / div

V9a (YUV DEC)
0.2V / div AC
10µs / div

V12 (FSUB_COMB ON/OFF)
0.1V / div AC
0.5µs / div

I2 (IF1)
50mV / div DC
50µs / div

A8 (A
(volume
0V2
0.5

S4(SC_1FH)
1V / div DC
10µs / div

V2 (HEATER)
5V / div DC
5µs / div

V5c (YUV IC7500)
0.2V / div AC
10µs / div

V9b (YUV DEC)
0.2V / div AC
10µs / div

V13 (SYS 1)
PAL BG = 0V
NTSC M = 5V

I7 (AGC)
1V9 DC

A9 (A
-1KHz r
0V2
0.1

VERTICAL
(FRAME)

AUDIO

F1 (LV+)
10V / div DC
5ms / div

S5 (HA)
1V / div DC
10µs / div

V3a (RGB cathodes)
20V / div AC
10µs / div

V6 (SC_2FH)
1V / div DC
10µs / div

V9c (YUV DEC)
0.2V / div AC
10µs / div

V15a (Y/CVBS_MAIN)
0.2V / div AC
10µs / div

A1 (AUDIO AMP. OUT R)
-1KHz right (incr.volume)
0V2 / div AC
0.1ms / div

A10 (A
-1KHz r
0V2
0.1

F2 (+13V-LOT)
5V / div DC
5ms / div

S6 (HD)
1V / div DC
10µs / div

V3b (RGB cathodes)
20V / div AC
10µs / div

V7a (YUV FBX)
0.2V / div DC
10µs / div

V10a (Y/CVBS_COMB)
0.2V / div AC
10µs / div

V15b (C/CVBS_MAIN)
0.2V / div AC
10µs / div

A2(AUDIO AMP. OUT L)
-3KHz left (incr.volume)
0V2 / div AC
0.2ms / div

A11 (
27V

F3 (-15V-LOT)
5V / div DC
5ms / div

S7 (VD)
1V / div DC
5ms / div

V3c (RGB cathodes)
20V / div AC
10µs / div

V7b (YUV FBX)
0.2V / div DC
10µs / div

V10b (C/CVBS_COMB)
0.2V / div DC
10µs / div

V16 (CVBS)
0.2V / div AC
10µs / div

A3 (SOUND_SUP)
29V5 DC

A12 (
(volume
0V2
0.5

S8 (SC_2FH)
1V / div DC
10µs / div

V4a (RGB IC7500)
1V / div DC
10µs / div

V7c (YUV FBX)
0.2V / div AC
10µs / div

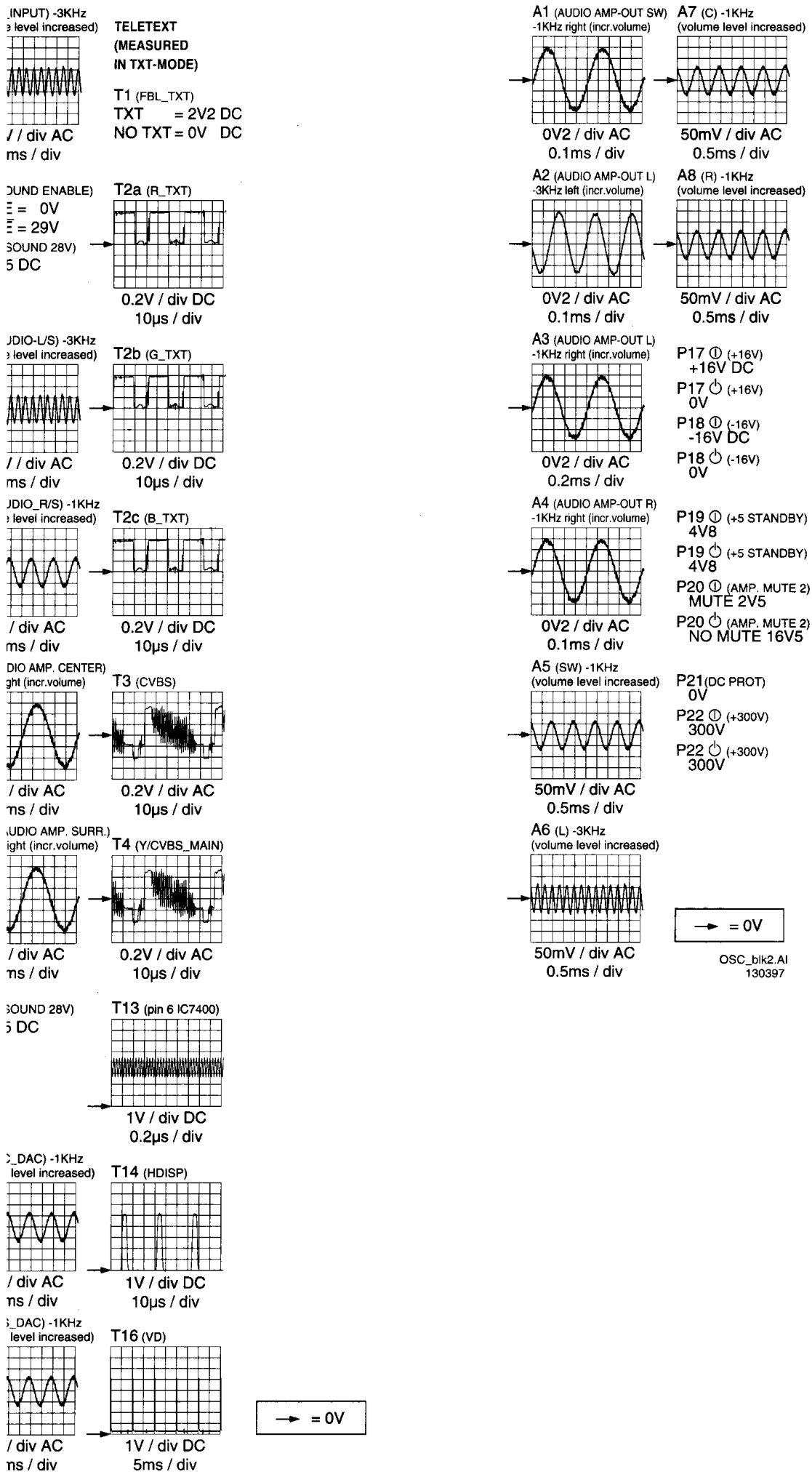
V11a -(R-Y)
0.2V / div AC
20µs / div

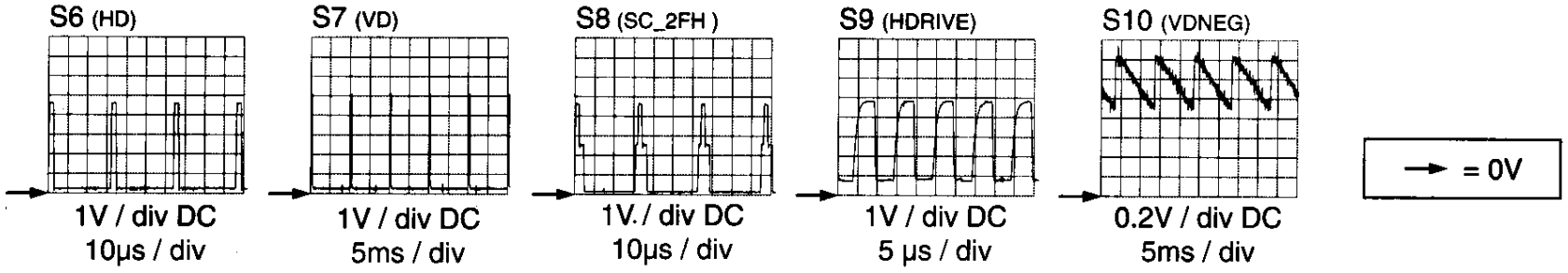
V17 (CVBS_TERR)
0.5V / div DC
10µs / div

A4 (R_INPUT) -1KHz
(volume level increased)
0V2 / div AC
0.5ms / div

A13 (S
(volume
0V2
0.5

Vue d'ensemble des oscillogrammes





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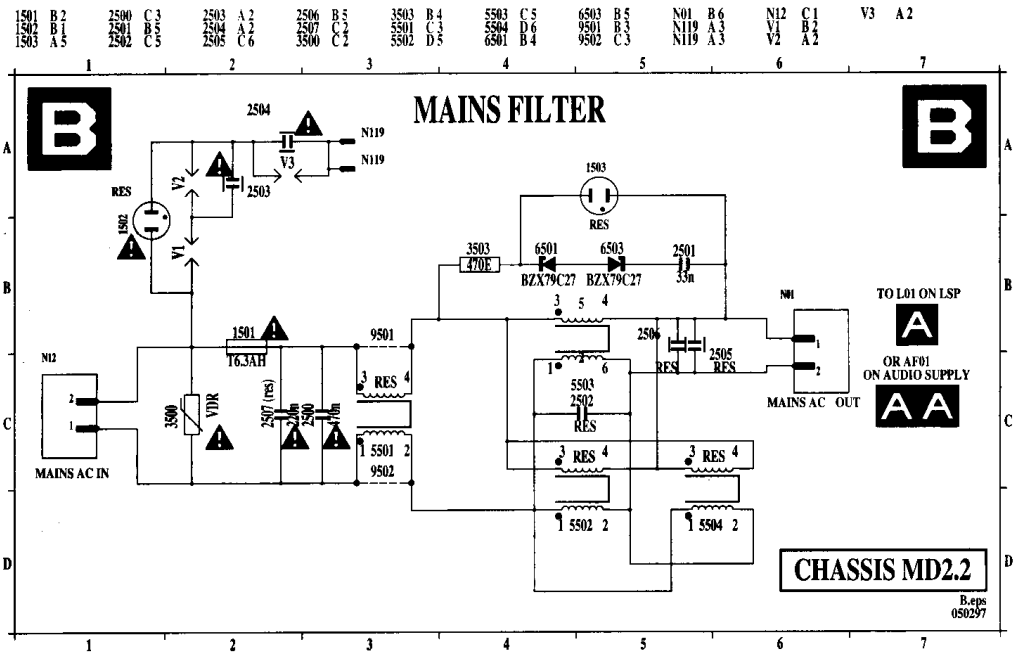
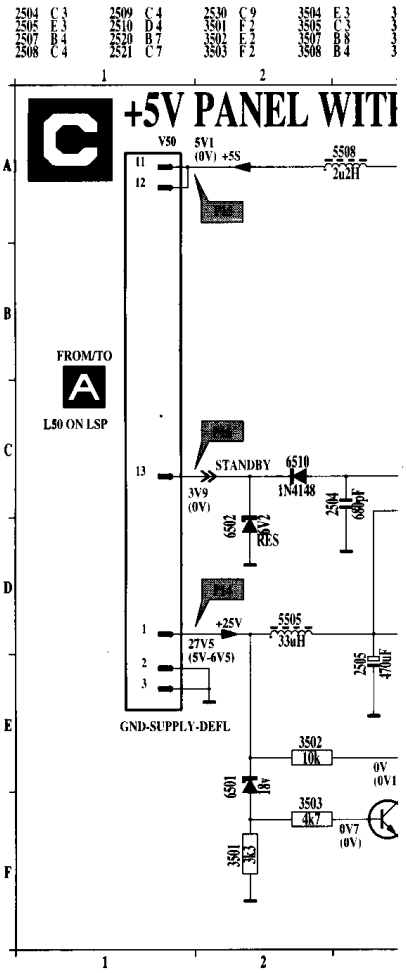
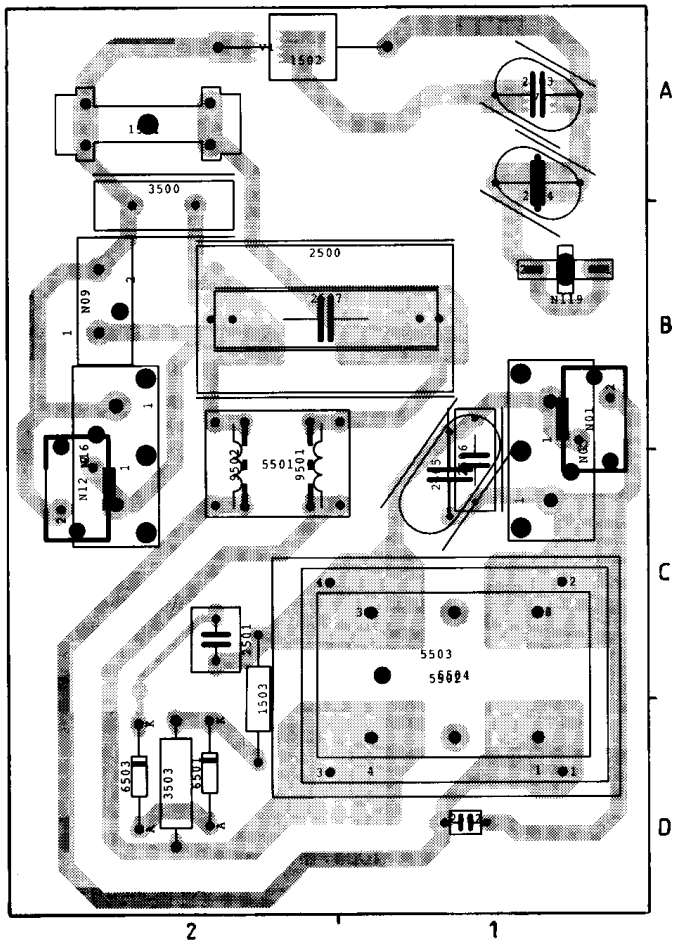
See appendix for circuit diagram LSP & SSP & DDP

Mains filter panel / Netzfilterplatine / Platine filtre d'alimentation



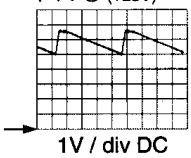


1501 A 2	2500 B 2	2503 A 1	2506 C 1	3503 D 2	5503 D 1	6503 D 2	N01 B 1	N12 C 2
1502 A 1	2501 C 2	2504 A 1	2507 B 2	5501 B 2	5504 D 1	9501 B 2	N03 C 1	N16 B 2
1503 C 2	2502 D 1	2505 C 1	3500 B 2	5502 D 1	6501 D 2	9502 B 2	N09 B 2	N119 B 1



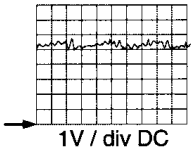
P14 ① (+25V)
27V5 DC

P14 ⏻ (+25V)



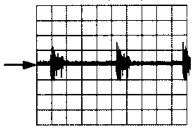
1V / div DC
0.1s / div

P15 ① (+5S)



1V / div DC
10µs / div

P15 ⏻ (+5S)



0.1V / div DC
0.1s / div

→ = 0V

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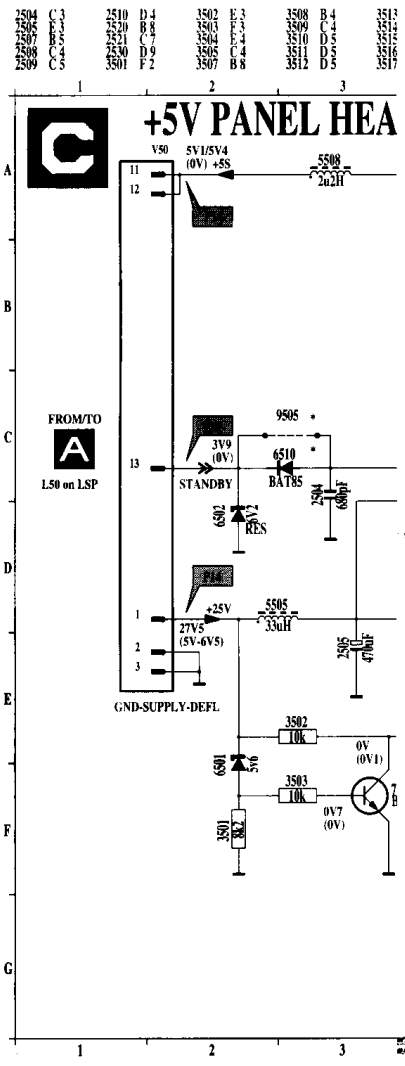
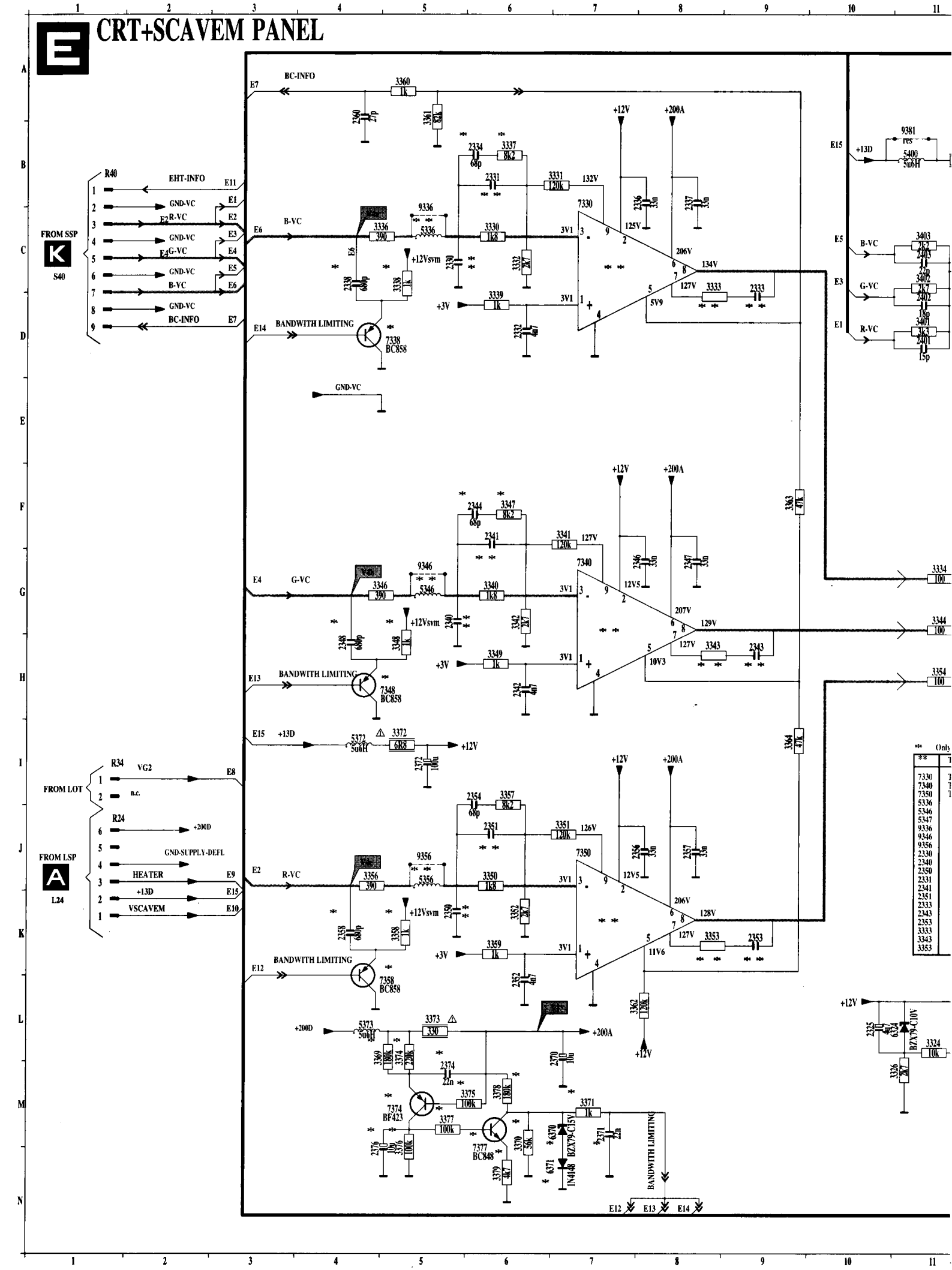
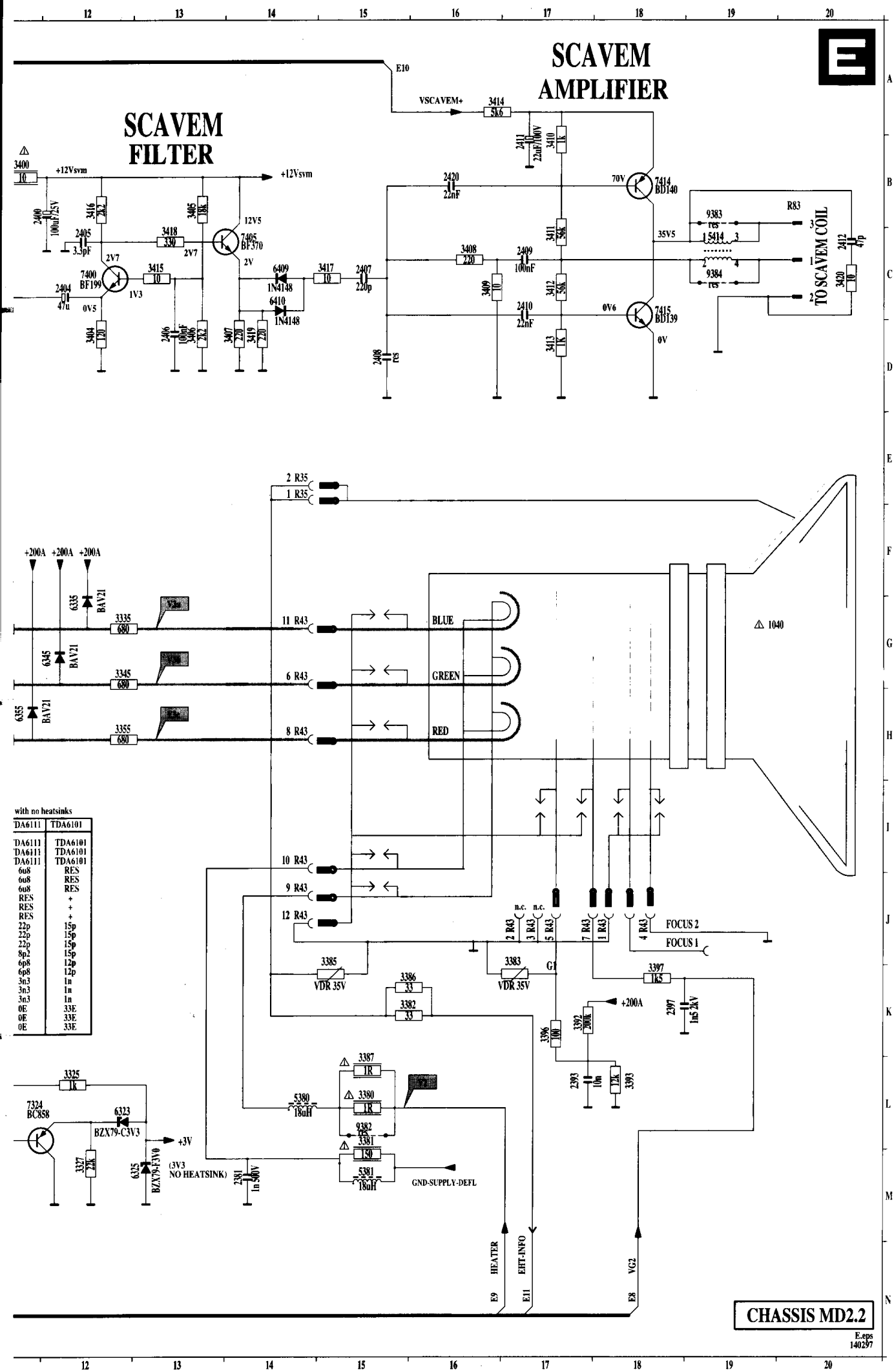


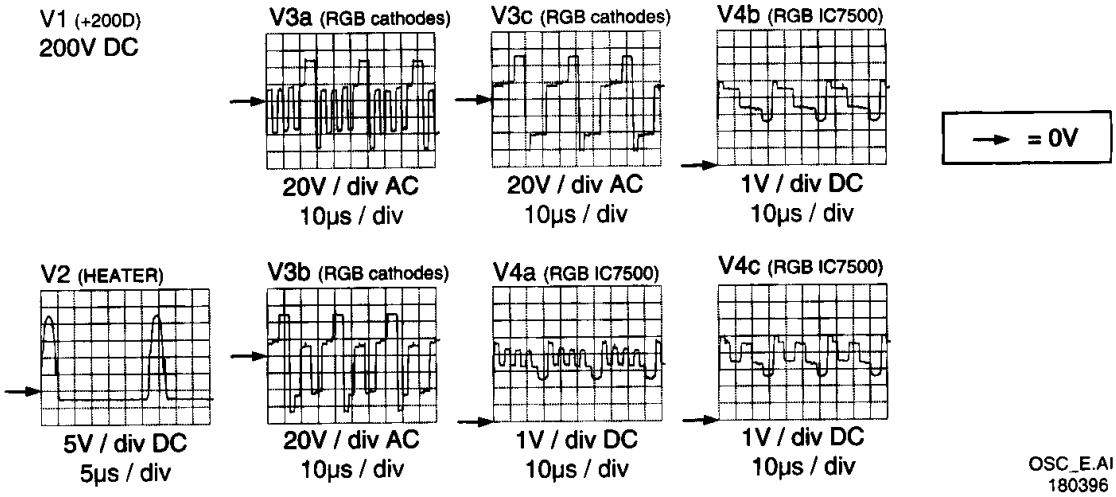
| | | |


E
CRT+SCAVEM PANEL
FROM SSP
K
S40
R40
EHT-INFO
GND-VC
R-VC
G-VC
B-VC
BC-INFO
FROM LOT
R34
VG2
n.c.
R24
+200D
FROM LSP
A
L24
GND-SUPPLY-DEFL
HEATER
+13D
VSCAVEM
BC-INFO
B-VC
G-VC
R-VC
BANDWITH LIMITING
7338 BC858
7348 BC858
7358 BC858
7330
7340
7350
+12V
+200A
+12Vsvm
+3V
+200D
+200A
7374 BF423
7377 BC848
BZX79-C15V
1N4148
BZX79-C10V
BANDWITH LIMITING
E12 E13 E14

Bildröhren & SCAVEM-Platine / Platine tube-image & SCAVEM



with no heatsinks	
TDA6111	TDA6101
TDA6111	TDA6101
TDA6111	TDA6101
TDA6111	TDA6101
6u8	RES
6u8	RES
6u8	RES
RES	+
RES	+
RES	+
22p	15p
22p	15p
22p	15p
8p2	15p
6p8	12p
6p8	12p
3n3	1n
3n3	1n
3n3	1n
0E	33E
0E	33E
0E	33E


V1 (+200D)
200V DC
V3a (RGB cathodes)
20V / div AC
10µs / div
V3c (RGB cathodes)
20V / div AC
10µs / div
V4b (RGB IC7500)
1V / div DC
10µs / div
= 0V
V2 (HEATER)
5V / div DC
5µs / div
V3b (RGB cathodes)
20V / div AC
10µs / div
V4a (RGB IC7500)
1V / div DC
10µs / div
V4c (RGB IC7500)
1V / div DC
10µs / div
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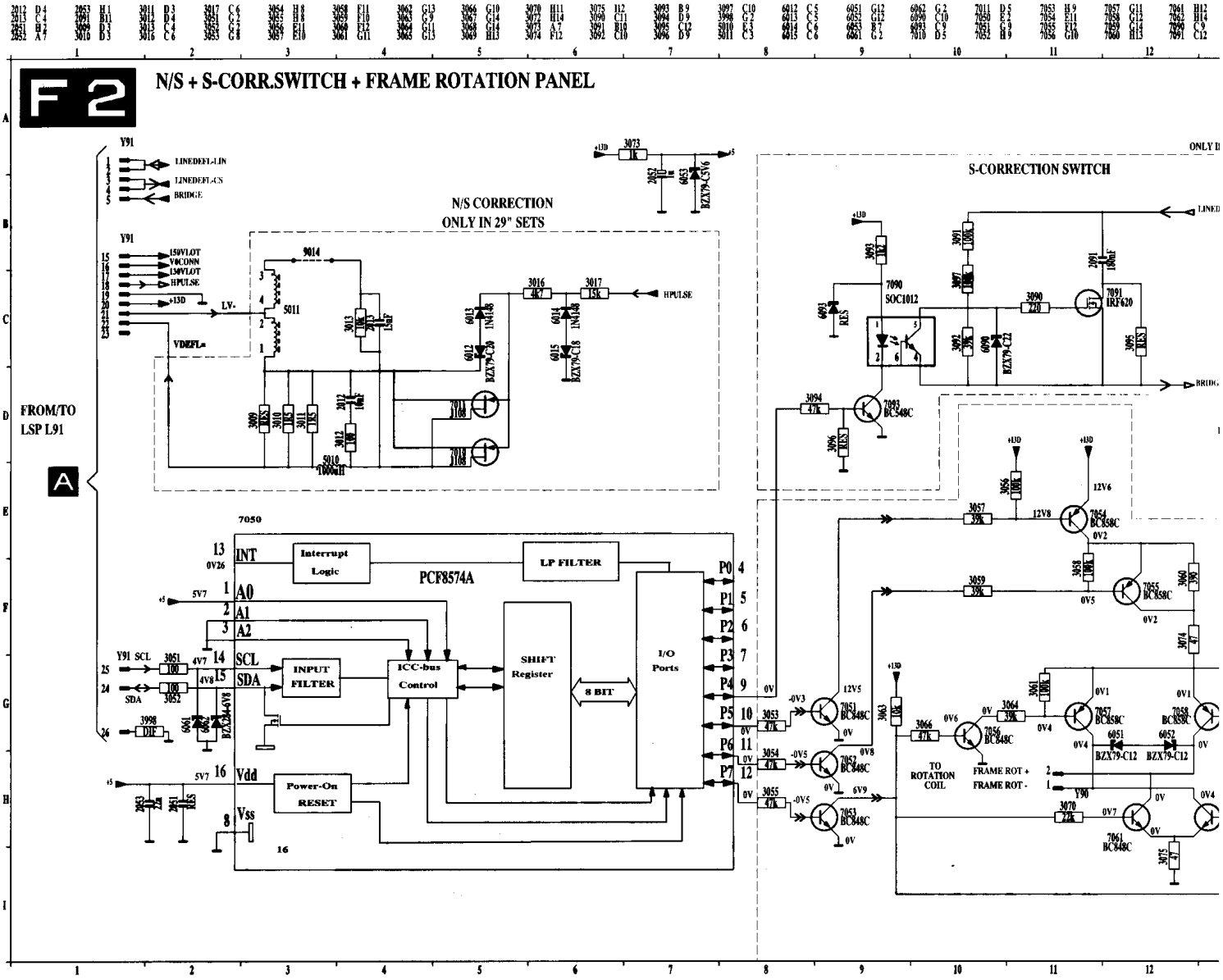
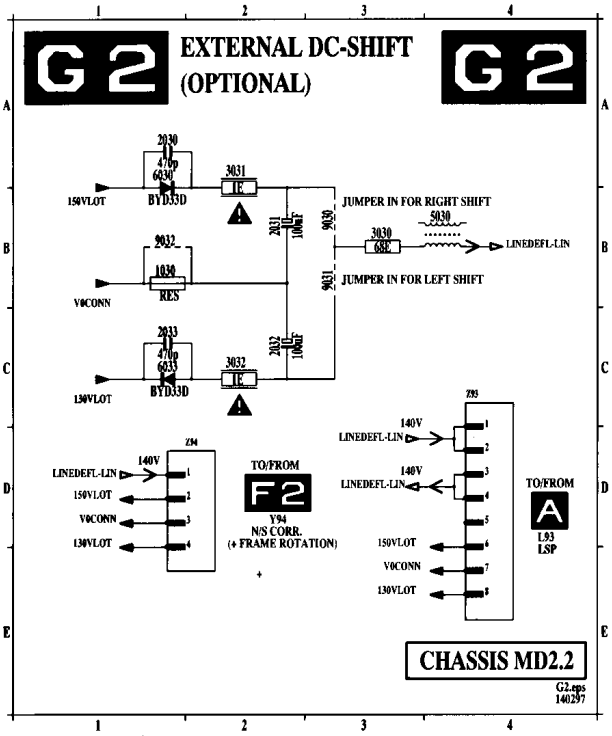
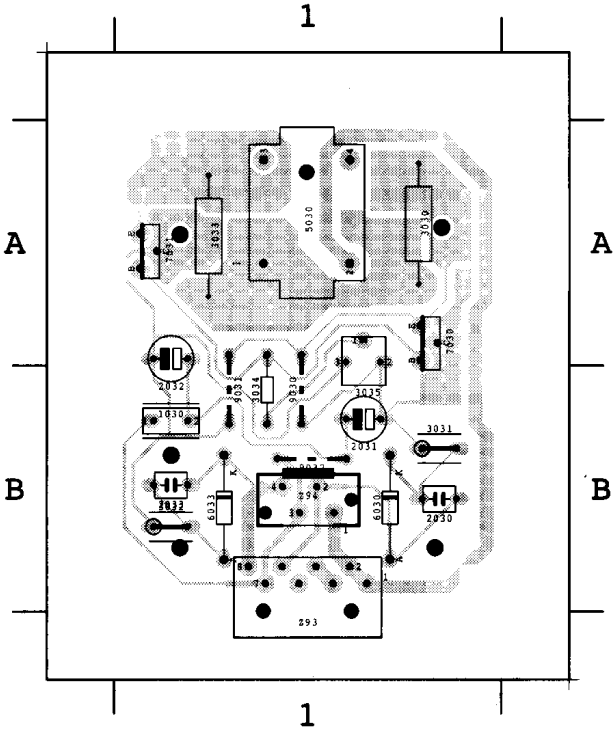
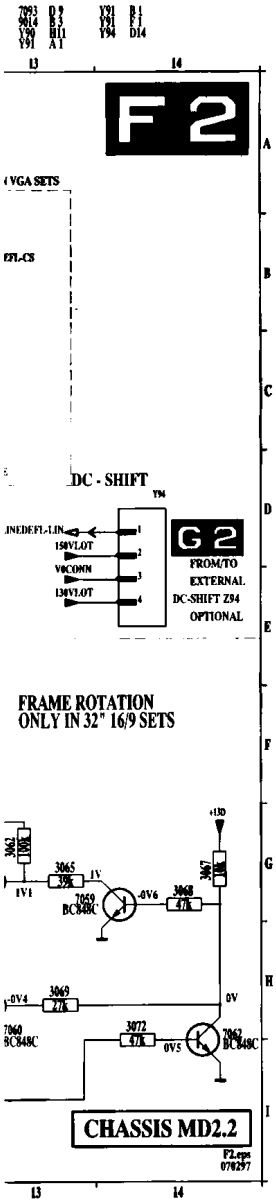
North/South + Frame rotation + S-correction panel / Nord/Süd + Drehrahmen + S-Korrekturplatine / Platine N/S + rotation de Trame + Correction S



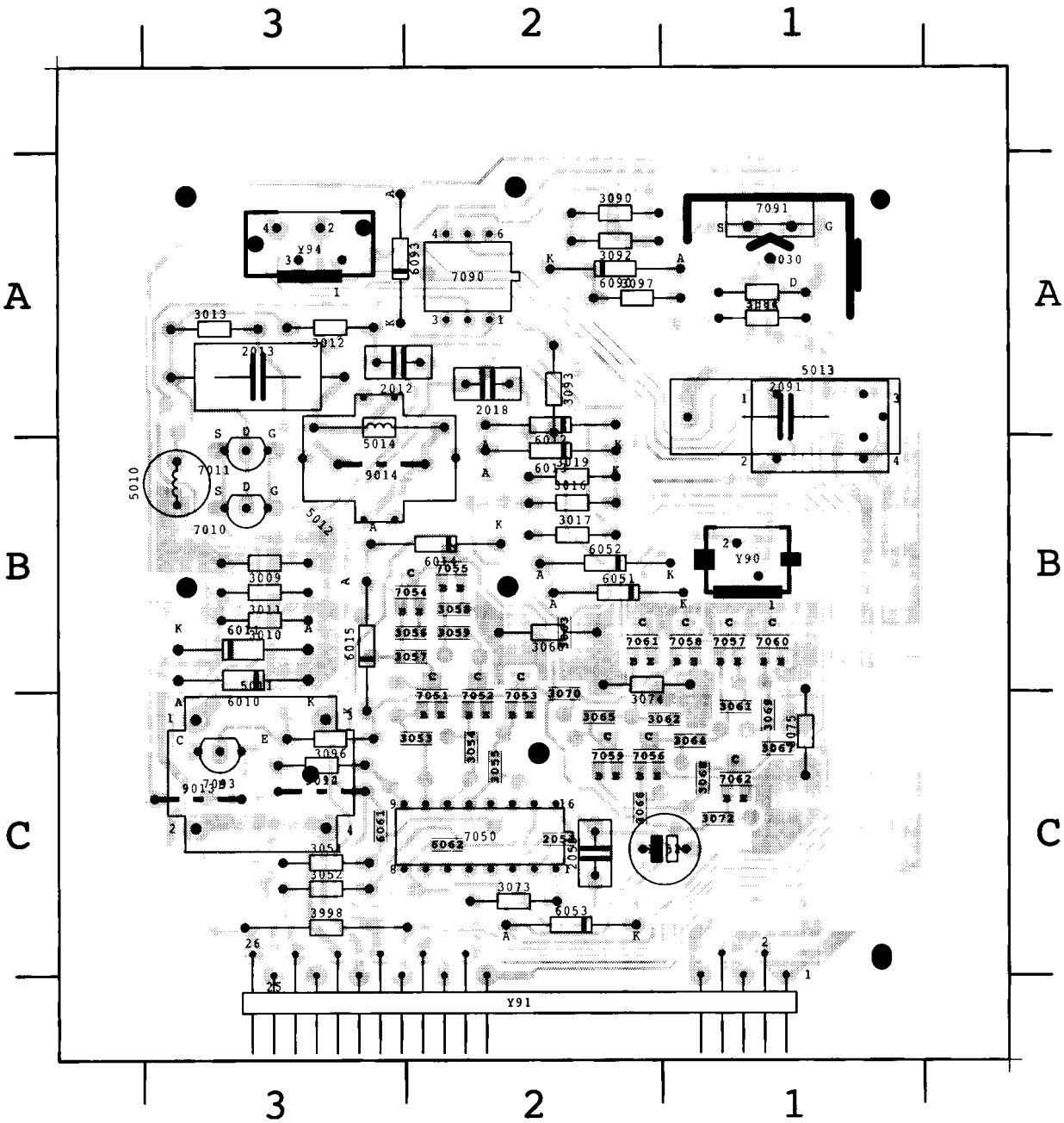




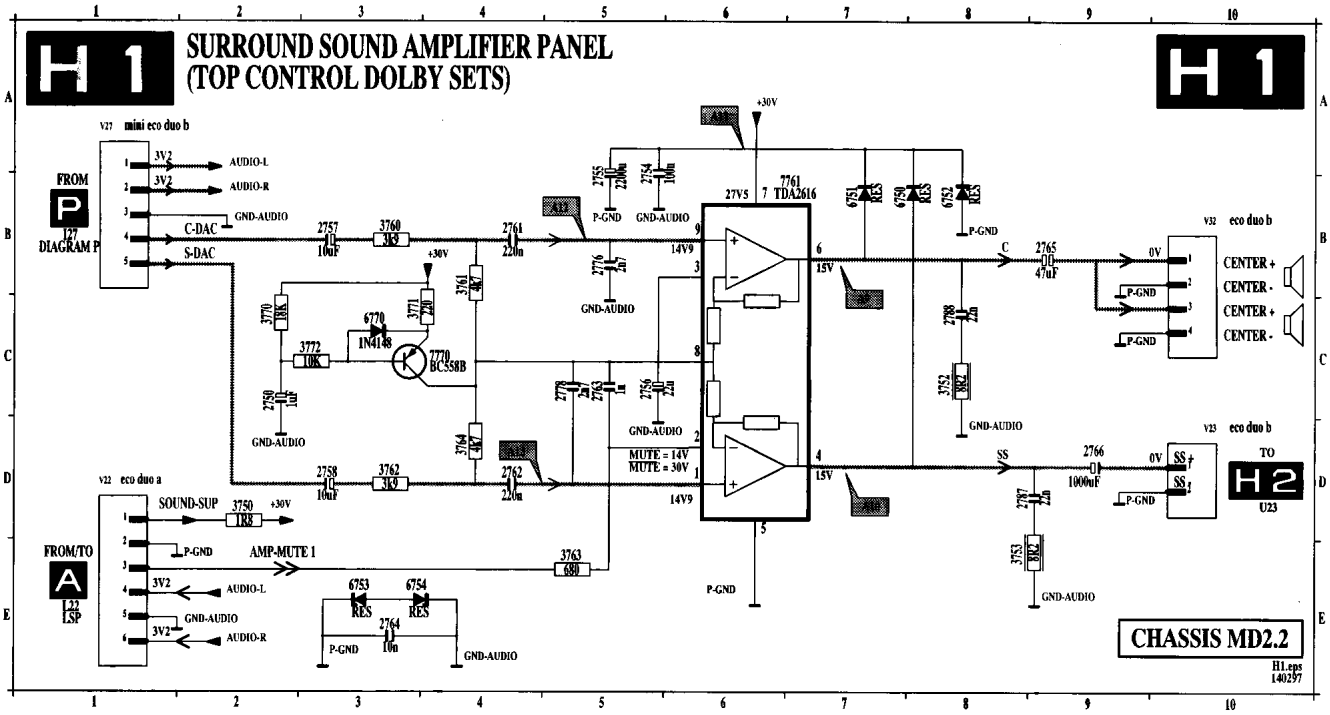
External DC shift panel / Externe-DC-verschiebungs-Platine / Platine déphasage externe CC



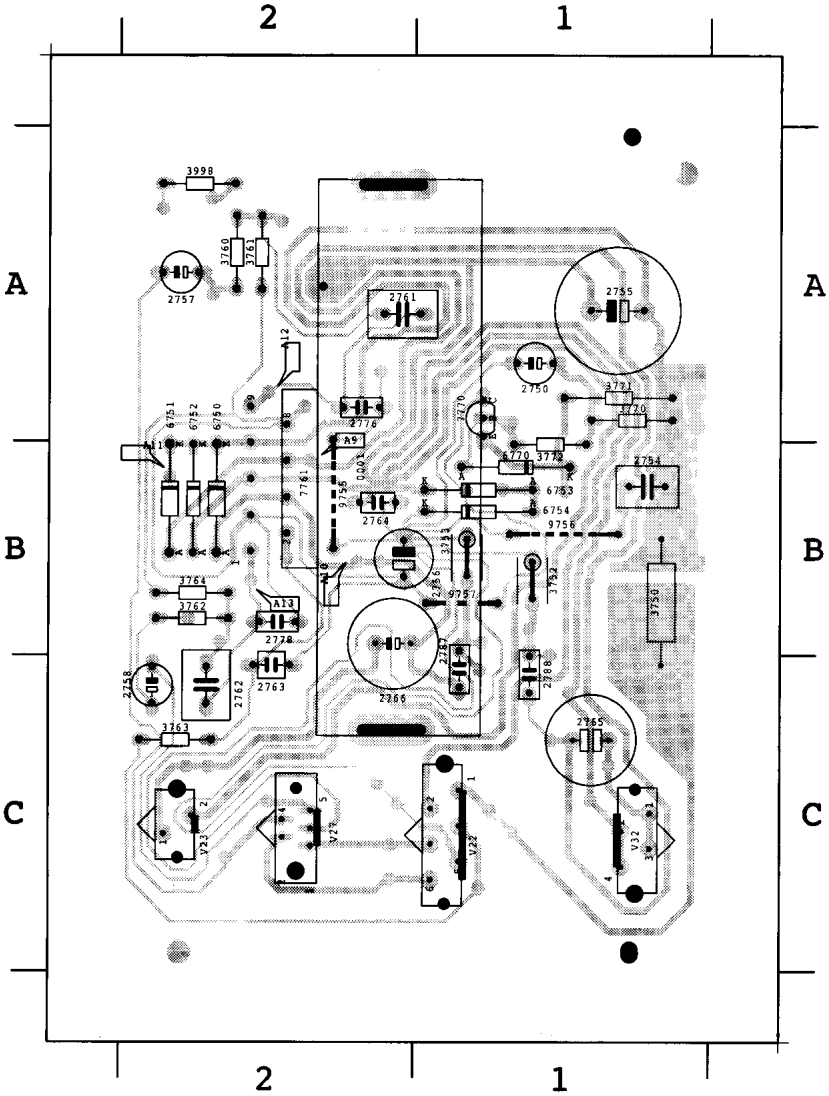
0030 A 1	3010 B 3	3053 C 2	3062 C 1	3072 C 1	3095 A 1	6010 B 3	6061 C 3	7053 C 2	7062 C 1	Y94 A 3
2012 A 2	3011 B 3	3054 C 2	3063 B 2	3073 C 2	3096 C 3	6011 B 3	6062 C 2	7054 B 2	7090 A 2	
2013 A 3	3012 A 3	3055 C 2	3064 C 1	3074 B 1	3097 A 2	6012 A 2	6090 A 1	7055 B 2	7091 A 1	
2018 A 2	3013 A 3	3056 B 2	3065 C 2	3075 C 1	3998 C 3	6013 B 2	6093 A 3	7056 C 2	7093 C 3	
2051 C 2	3016 B 2	3057 B 2	3066 C 2	3090 A 2	5010 B 3	6014 B 3	7010 B 3	7057 B 1	9012 C 3	
2052 C 1	3017 B 2	3058 B 2	3067 C 1	3091 A 1	5011 C 3	6015 B 3	7011 B 3	7058 B 1	9013 C 3	
2053 C 2	3019 B 2	3059 B 2	3068 C 1	3092 A 2	5012 A 3	6051 B 2	7050 C 2	7059 C 2	9014 B 2	
2091 A 1	3051 C 3	3060 B 2	3069 C 1	3093 A 2	5013 A 1	6052 B 2	7051 C 2	7060 B 1	Y90 B 1	
3009 B 3	3052 C 3	3061 C 1	3070 C 2	3094 C 3	5014 A 2	6053 C 2	7052 C 2	7061 B 2	Y91 C 1	

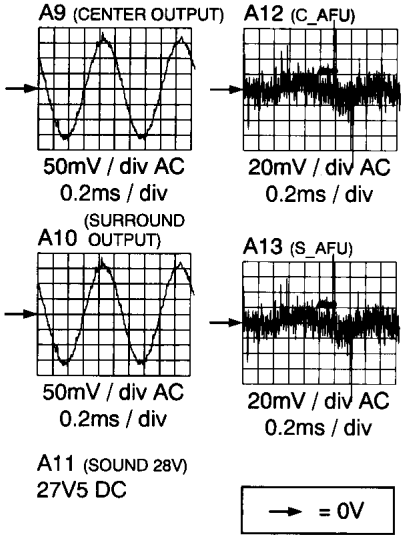


Surround sound panel / Surround Sound-Platine / Platine son Surround



0001 A 2	2757 A 2	2764 B 2	2787 B 1	3760 A 2	3770 A 1	6751 B 2	7761 B 2	V22 C 1
2750 A 1	2758 C 2	2765 C 1	2788 C 1	3761 A 2	3771 A 1	6752 B 2	7770 A 1	V23 C 2
2754 B 1	2761 A 2	2766 B 2	3750 C 1	3762 B 2	3772 B 1	6753 B 1	9755 B 2	V27 C 2
2755 A 1	2762 C 2	2776 A 2	3752 B 1	3763 C 2	3998 A 2	6754 B 1	9756 B 1	V32 C 1
2756 B 2	2763 C 2	2778 B 2	3753 B 1	3764 B 2	6750 B 2	6770 B 1	9757 B 1	





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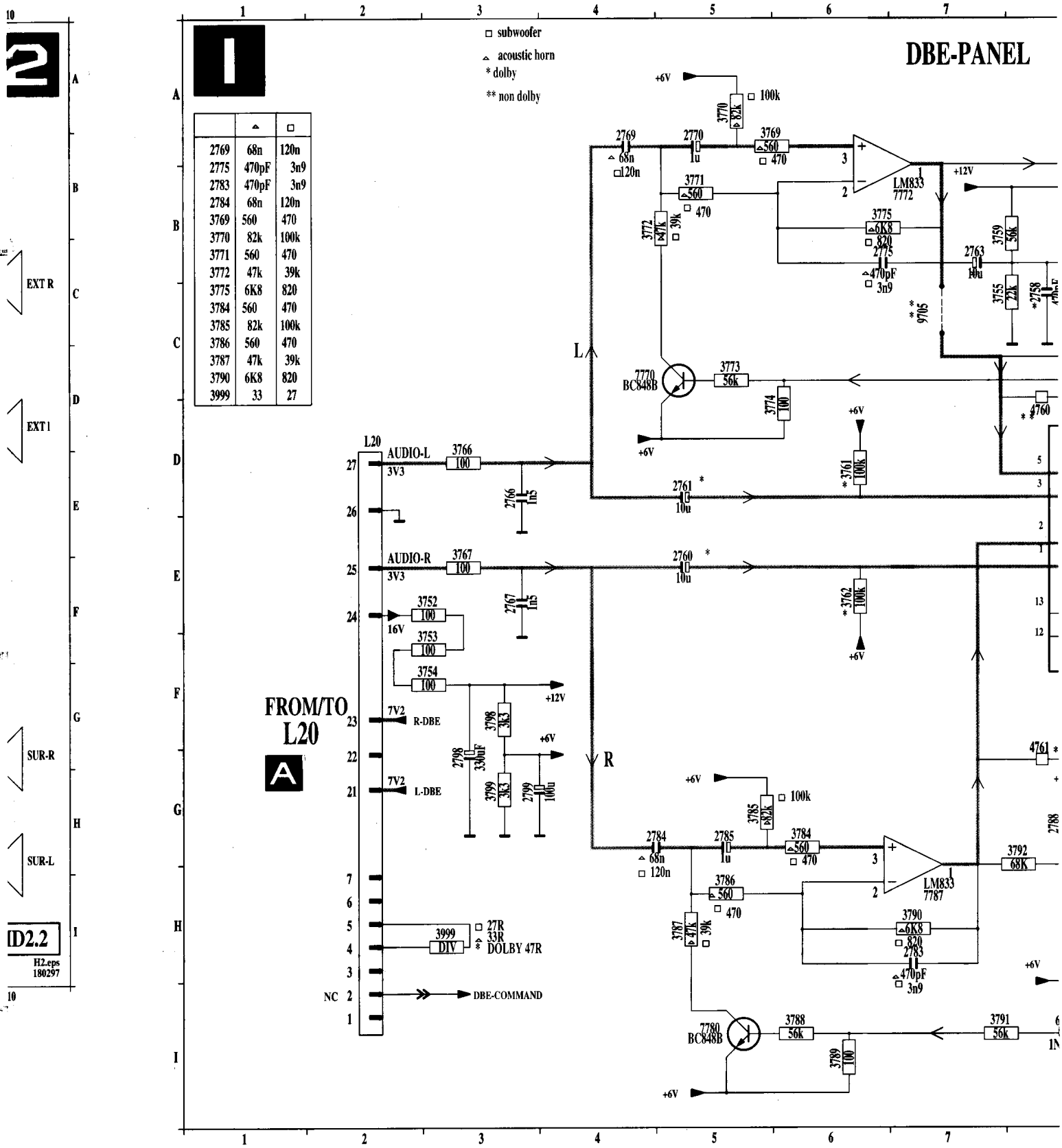
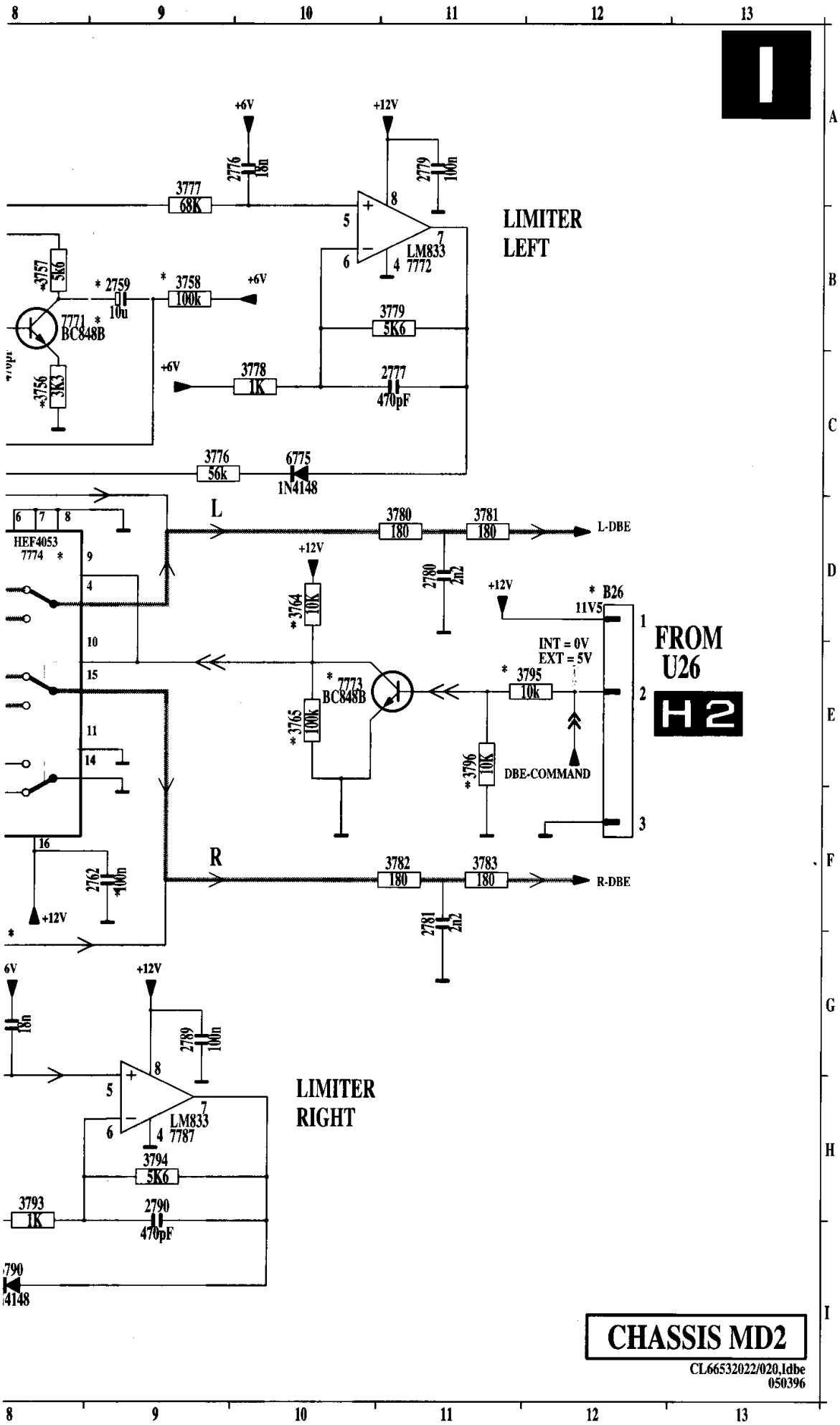
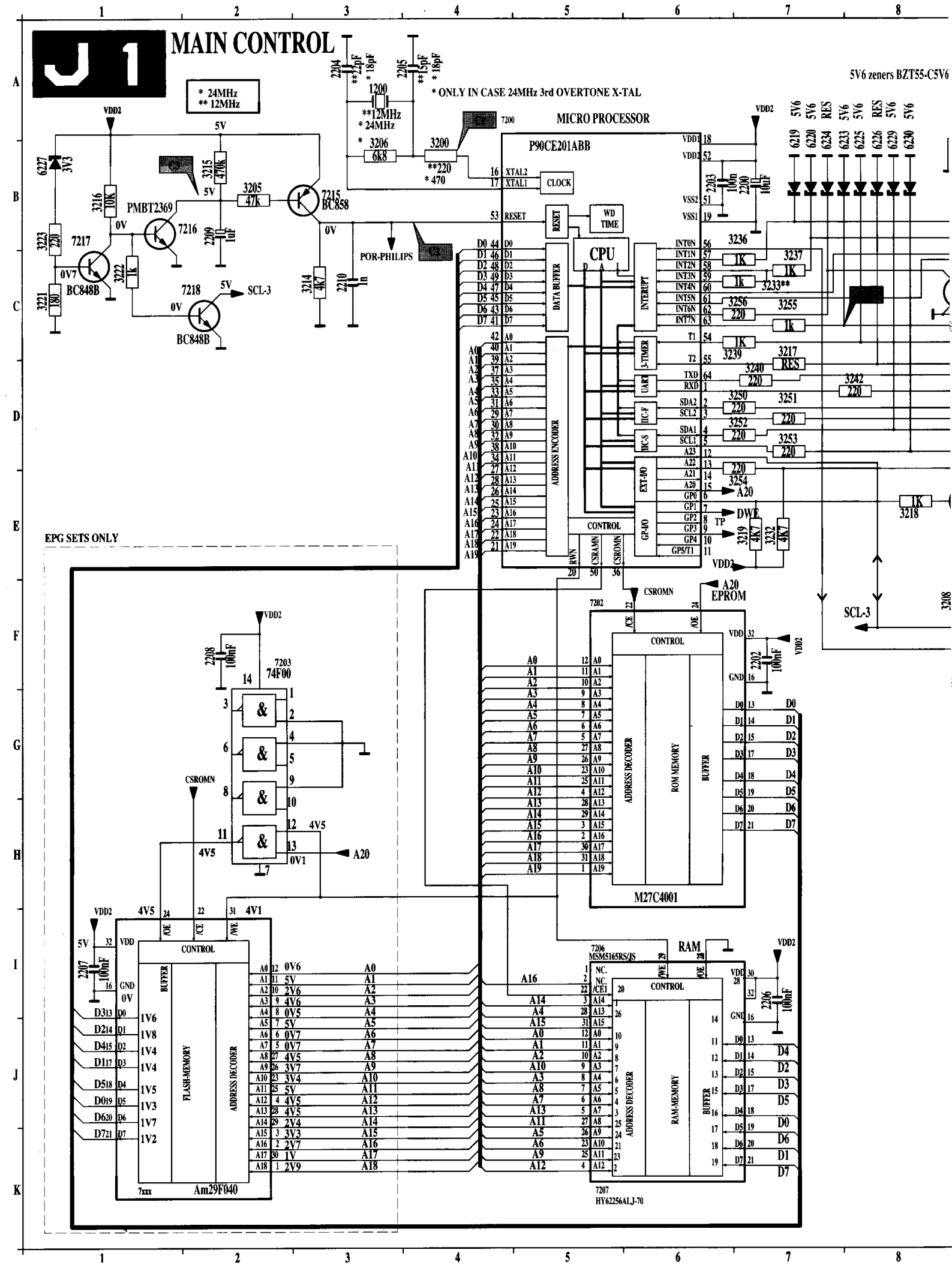
DBE (Dynamic Bass Enhancement) panel / DBE Dynamic Bass Enhancement)-Platine

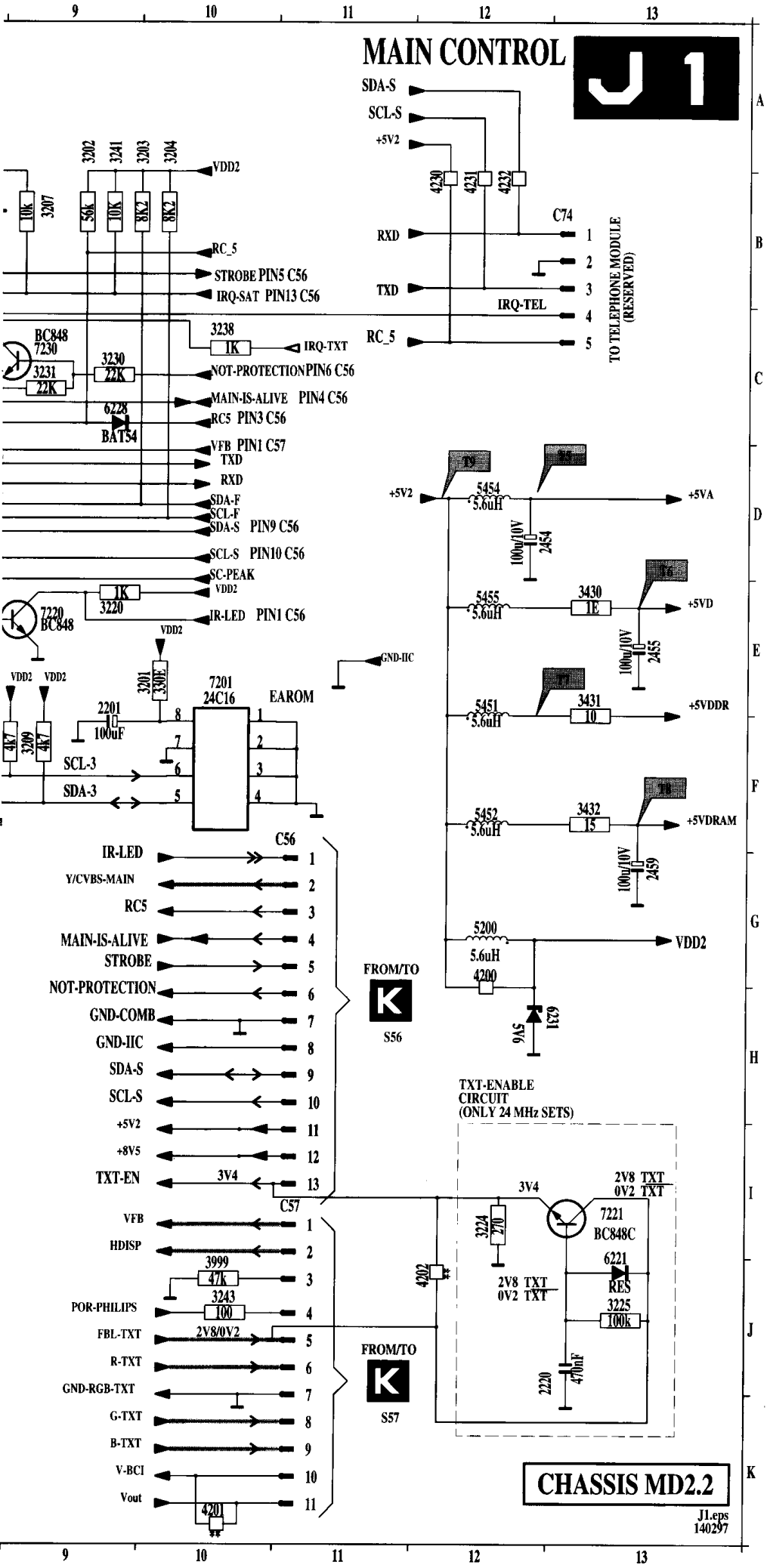


	△	□
2769	68n	120n
2775	470pF	3n9
2783	470pF	3n9
2784	68n	120n
3769	560	470
3770	82k	100k
3771	560	470
3772	47k	39k
3775	6K8	820
3784	560	470
3785	82k	100k
3786	560	470
3787	47k	39k
3790	6K8	820
3999	33	27

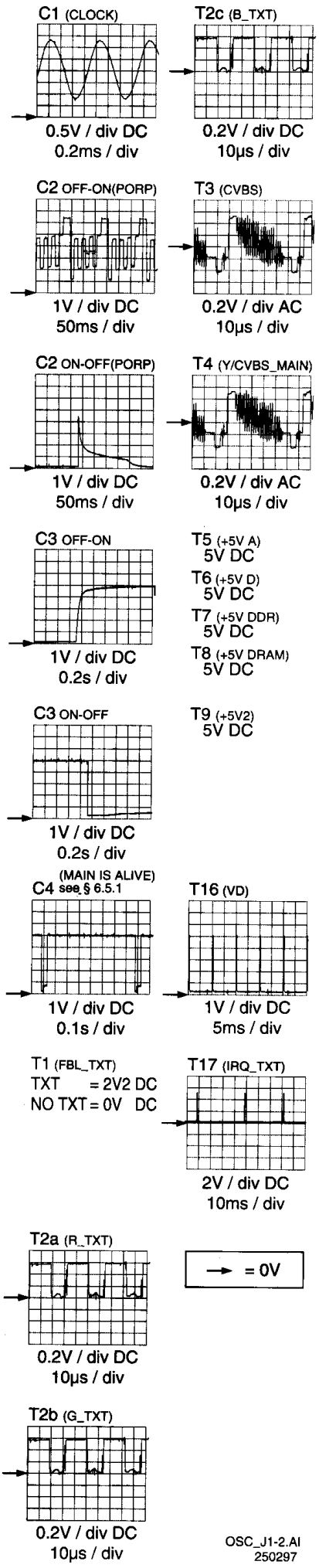
Platine DBE (Amélioration Dynamique des Basses

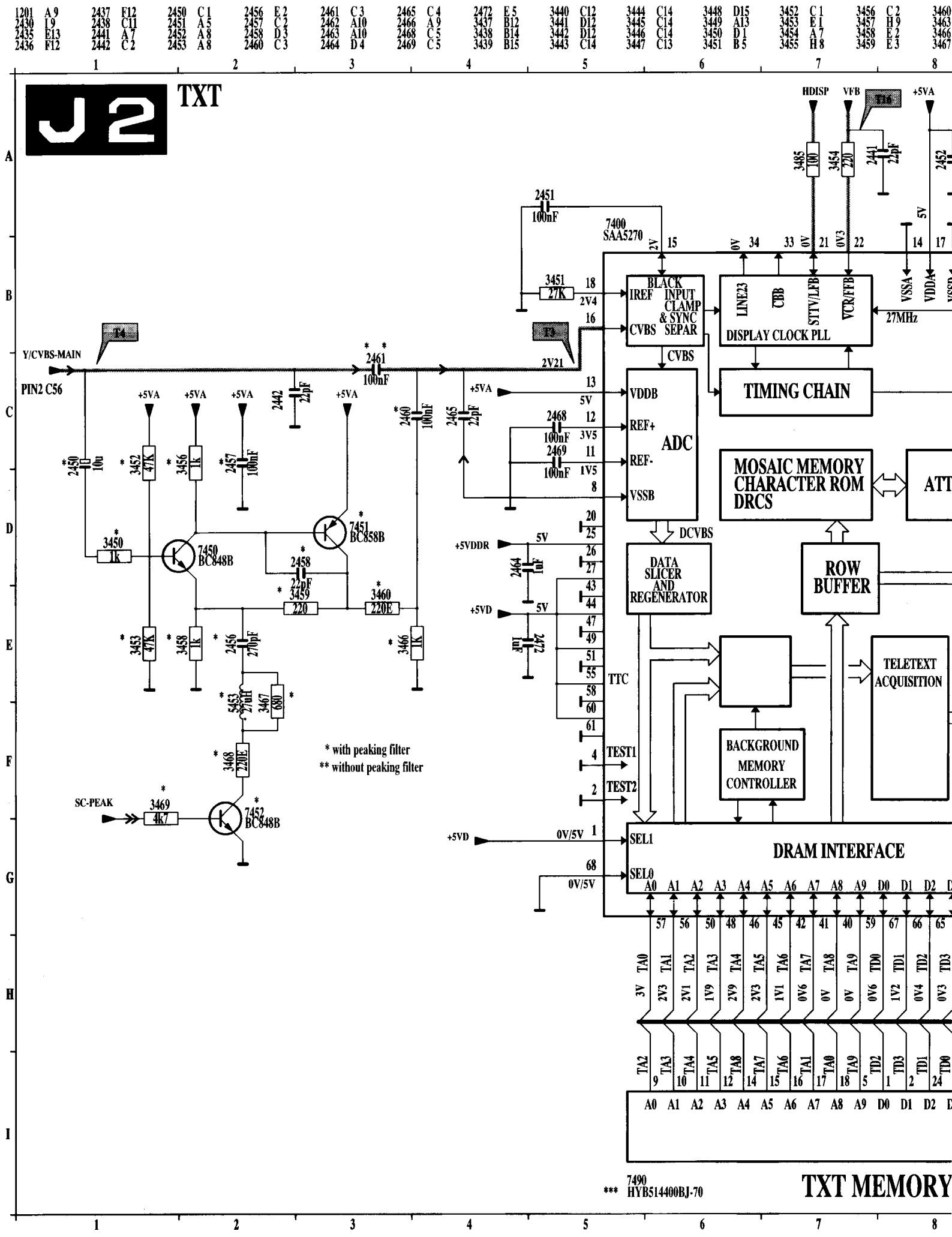



J 1
MAIN CONTROL
* 24MHz
** 12MHz
* ONLY IN CASE 24MHz 3rd OVERTONE X-TAL
5V6 zeners BZT55-C5V6
MICRO PROCESSOR
P90CE201ABB
CLOCK
RESET
WD TIME
CPU
DATA BUFFER
ADDRESS ENCODER
CONTROL
INTERUPT
3-TIMER
UART
IIC-F
IICS
EXT-I/O
GP-I/O
POR-PHILIPS
PMBT2369
BC858
BC848B
SCL-3
EPG SETS ONLY
74F00
EPROM
M27C4001
ADDRESS DECODER
ROM MEMORY
BUFFER
RAM
MSM5165RS/JS
RAM-MEMORY
FLASH-MEMORY
Am29F040
HY62256ALJ-70



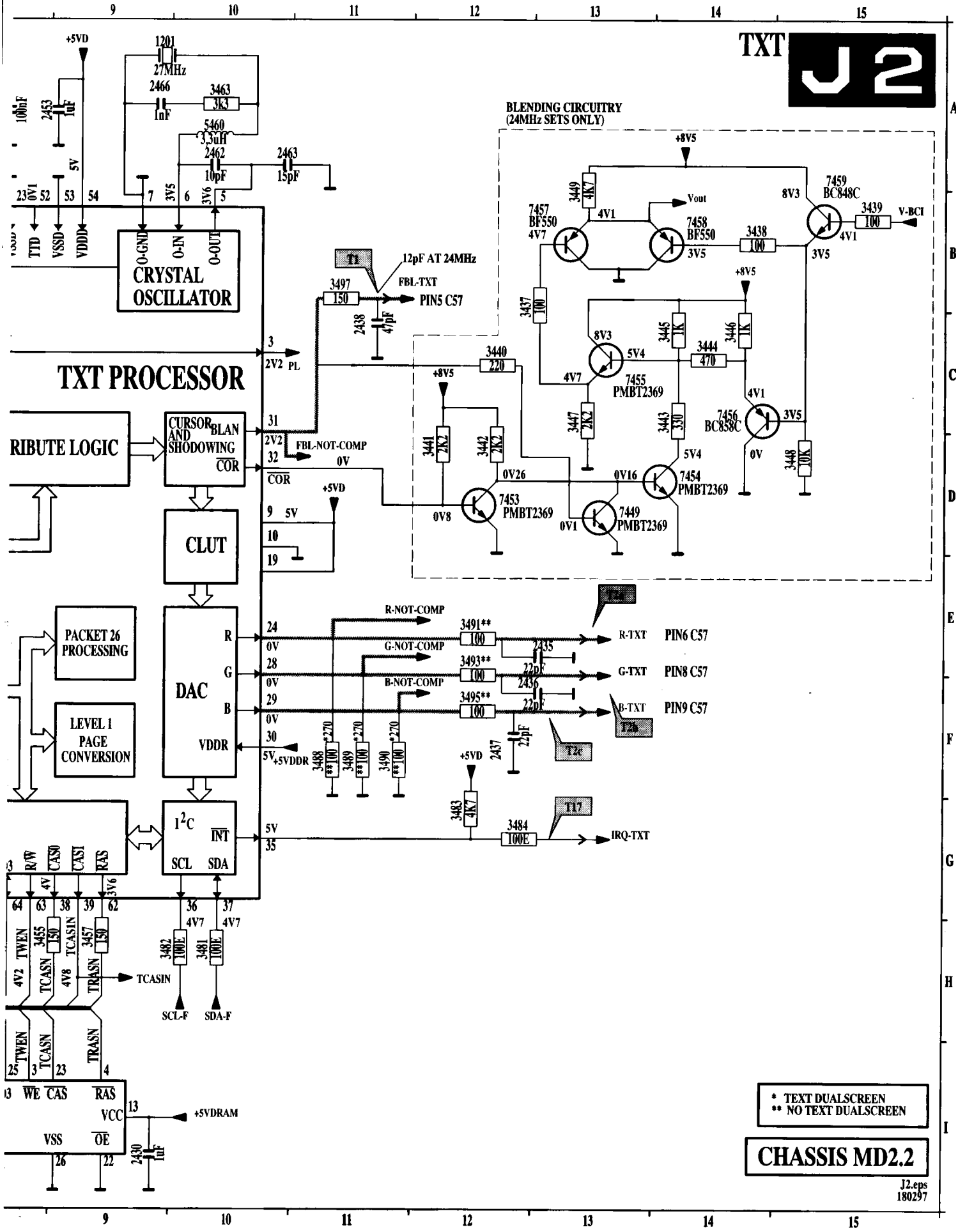
1200	A 3
2200	B 7
2201	E 9
2202	F 7
2203	B 6
2204	A 3
2205	A 4
2206	I 7
2207	I 1
2208	F 2
2209	B 2
2210	C 3
2220	J13
2454	D12
2455	E13
2459	G13
3200	B 4
3201	E10
3202	A 9
3203	A10
3204	A10
3205	B 2
3206	B 3
3207	B 9
3208	F 8
3209	F 9
3214	C 3
3215	B 2
3216	B 1
3217	C 7
3218	E 8
3219	E 7
3220	E 9
3221	C 1
3222	C 1
3223	B 1
3224	I12
3225	J13
3230	C 9
3231	C 9
3232	E 7
3233	C 7
3236	B 7
3237	C 7
3238	C10
3239	C 7
3240	D 7
3241	A 9
3242	D 8
3243	J10
3250	D 7
3251	D 7
3252	D 7
3253	D 7
3254	E 7
3255	C 7
3256	C 7
3430	E13
3431	E13
3432	F13
3999	J10
4200	G12
4201	K10
4202	J12
4230	B12
4231	B12
4232	B12
5200	G12
5451	E12
5452	F12
5454	D12
5455	E12
6219	A 7
6220	A 7
6221	J13
6225	A 8
6226	A 8
6227	B 1
6228	C 9
6229	A 8
6230	A 8
6231	H12
6233	A 8
6234	A 7
7200	A 4
7201	E10
7202	F 5
7203	F 3
7204	K 1
7206	I 5
7207	K 5
7215	B 3
7216	B 1
7217	B 1
7218	C 1
7220	E 9
7221	I13
7230	C 9
C56	F10
C57	I11
C74	B12

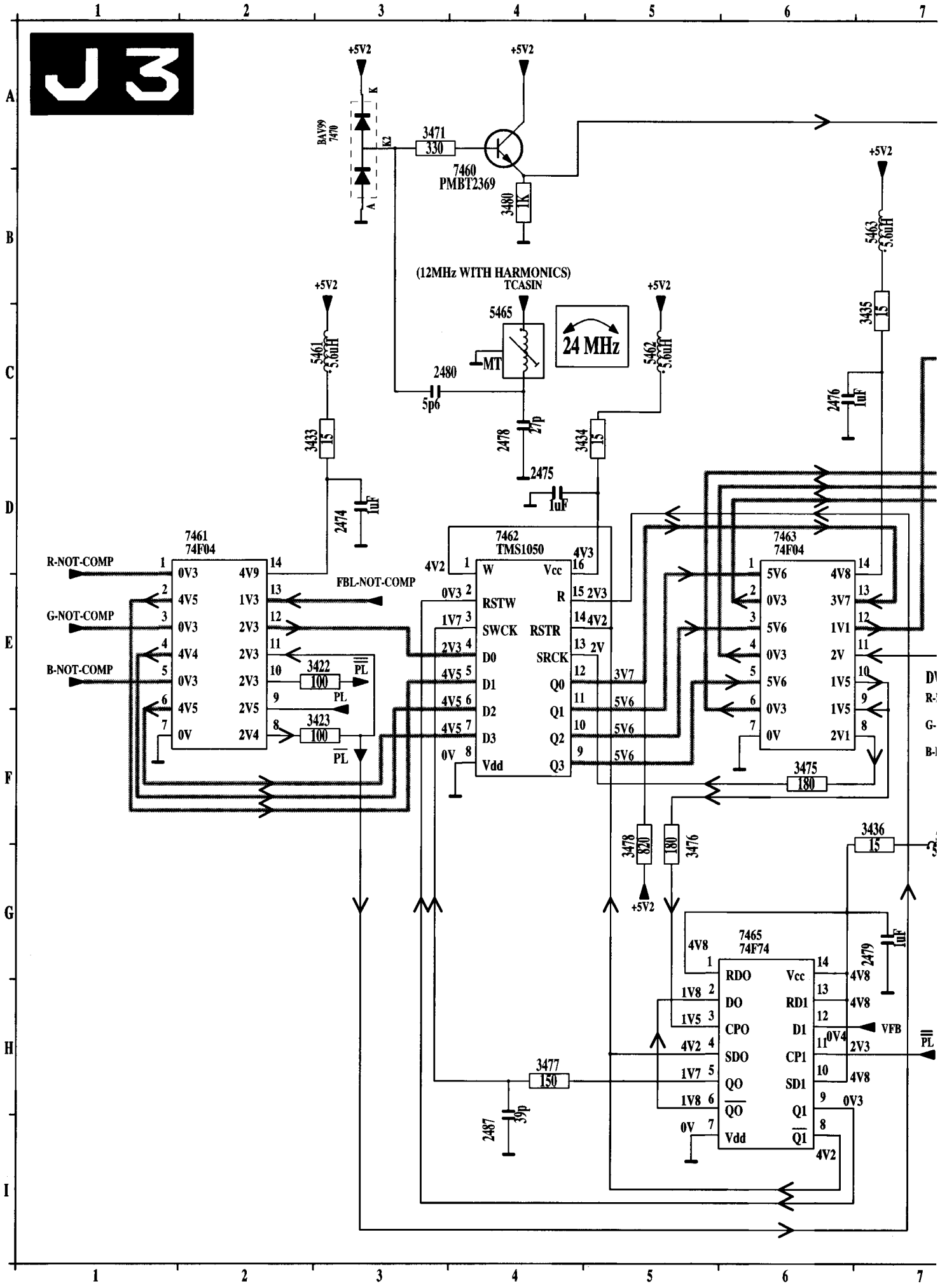



J2
TXT
Y/CVBS-MAIN
PIN2 C56
7400
SAA5270
BLACK
INPUT
CLAMP
& SYNC
SEPAR
IREF
CVBS
LINE23
CBB
STTV/LFB
VCR/FFB
DISPLAY CLOCK PLL
27MHz
TIMING CHAIN
VDDB
REF+
REF-
VSSB
ADC
MOSAIC MEMORY
CHARACTER ROM
DRCS
DCVBS
DATA
SLICER
AND
REGENERATOR
ROW
BUFFER
TELETEXT
ACQUISITION
BACKGROUND
MEMORY
CONTROLLER
TTC
TEST1
TEST2
SEL1
SEL0
DRAM INTERFACE
7450
BC848B
7451
BC858B
7452
BC848B
SC-PEAK
* with peaking filter
** without peaking filter
*** 7490
HYB514400BJ-70
TXT MEMORY

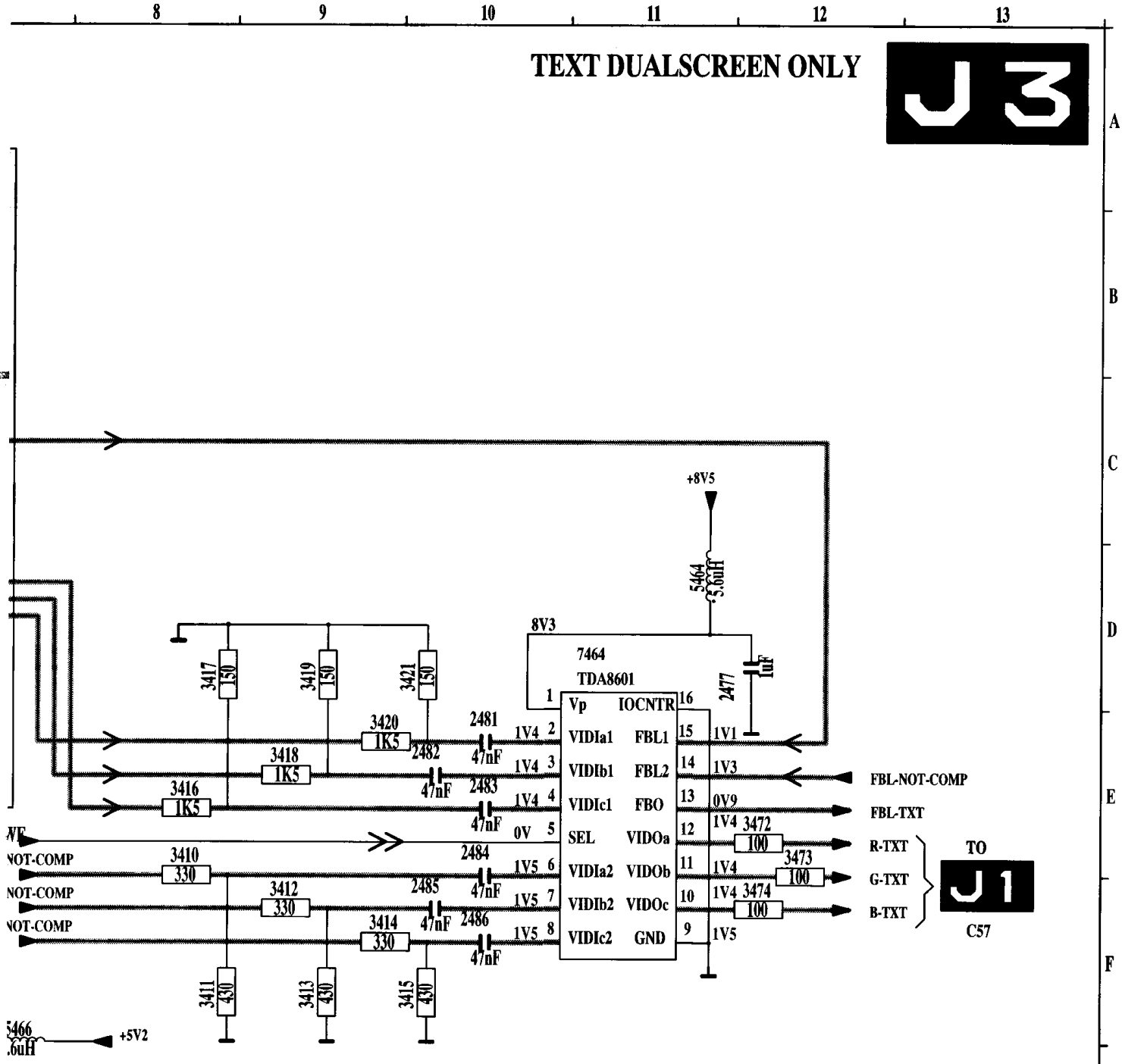
TXT & Control-Platine / Platine TXT & Commande

E 3	3468	F 2	3483	G12	3489	F11	3495*	F12	7400	A 5	7452	F 2	7456	C14	7490	I 5
A10	3469	F 1	3484	G12	3490	F11	3497	B11	7449	D13	7453	D12	7457	B12		
E 3	3481	H10	3485	A 7	3491*	E12	5453	E 2	7450	D 2	7454	D14	7458	B14		
E 2	3482	H10	3488	F11	3493*	E12	5460	A10	7451	D 3	7455	C13	7459	A15		




J3
+5V2
BAV99
7470
K
K2
A
3471
330
7460
PMBT2369
3480
1K
5463
5.6uH
3435
15
(12MHz WITH HARMONICS)
TCASIN
5465
MT
24 MHz
5461
5.6uH
5462
5.6uH
2480
5p6
2478
27p
2475
1uF
2476
1uF
3433
15
3434
15
2474
1uF
7461
74F04
R-NOT-COMP
G-NOT-COMP
B-NOT-COMP
FBL-NOT-COMP
0V3
4V9
4V5
1V3
0V3
2V3
4V4
2V3
0V3
2V3
4V5
2V5
0V
2V4
3422
100
3423
100
PL
7462
TMS1050
W
Vcc
RSTW
R
SWCK
RSTR
D0
SRCK
D1
Q0
D2
Q1
D3
Q2
Vdd
Q3
4V2
4V3
2V3
2V
3V7
5V6
7463
74F04
5V6
4V8
0V3
3V7
5V6
1V1
0V3
2V
5V6
1V5
0V3
1V5
0V
2V1
3475
180
3478
820
180
3476
3436
15
7465
74F74
RDO
Vcc
DO
RD1
CPO
D1
SDO
CP1
QO
SD1
QO
Q1
Vdd
Q1
4V8
1V8
1V5
4V2
1V7
1V8
0V
0V4
2V3
VFB
0V3
2479
1uF
3477
150
2487
39p

TXT & Control-Platine / Platine TXT & Commande



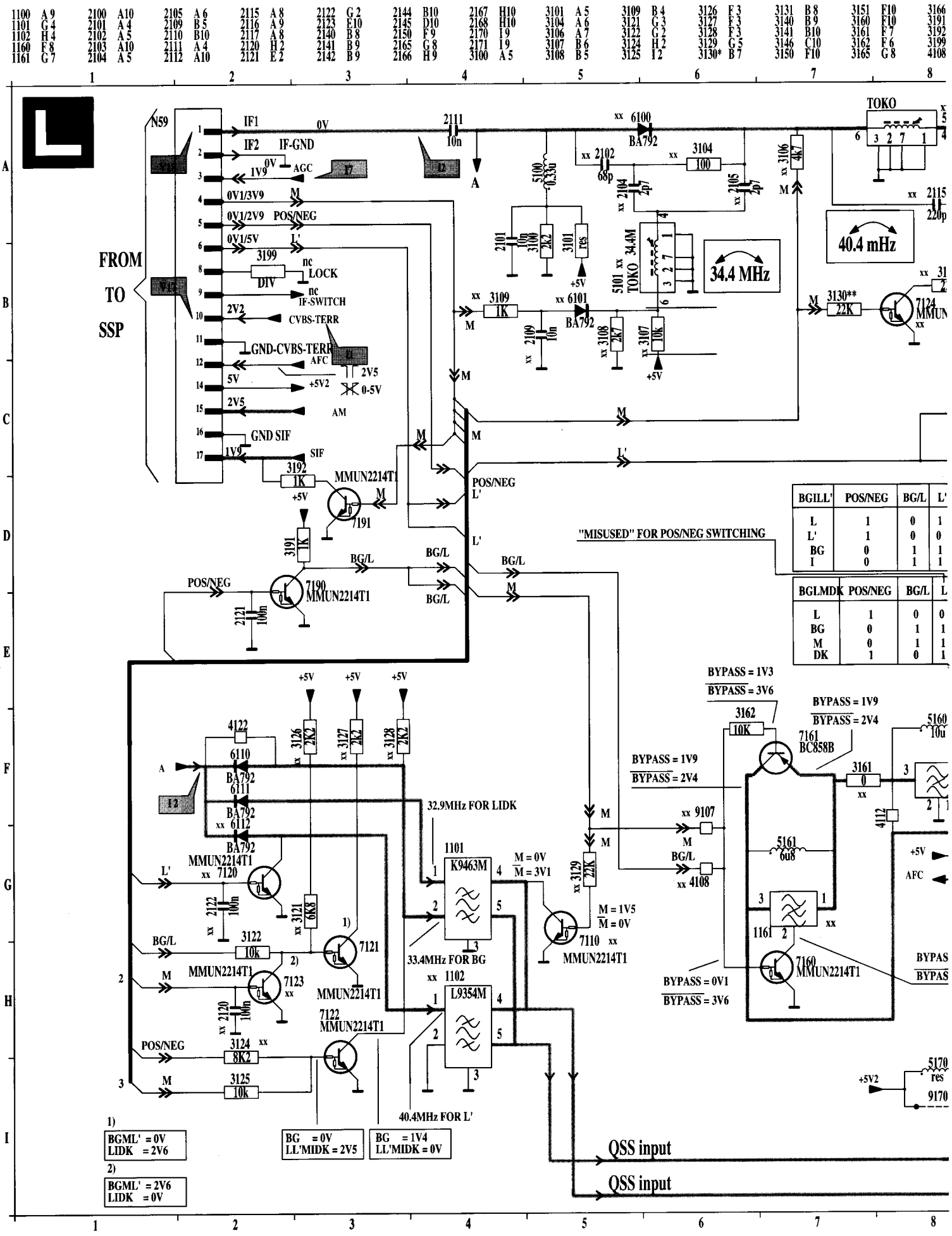
MEASURED IN TEXT DUALSCREEN MODE

2474	D3
2475	D4
2476	C6
2477	D11
2478	C4
2479	G7
2480	C3
2481	E10
2482	E10
2483	E10
2484	E10
2485	F10
2486	F10
2487	I4
3410	E8
3411	F8
3412	F9
3413	F9
3414	F9
3415	F10
3416	E8
3417	D8
3418	E9
3419	D9
3420	E9
3421	D10
3422	E3
3423	F3
3433	C3
3434	C5
3435	C7
3436	F7
3471	A3
3472	E12
3473	E12
3474	F12
3475	F6
3476	F5
3477	H4
3478	F5
3480	B4
5461	C3
5462	C5
5463	B7
5464	D11
5465	C4
5466	F7
7460	B4
7461	D2
7462	D4
7463	D6
7464	D11
7465	G6
7470	A3

CHASSIS MD2.2

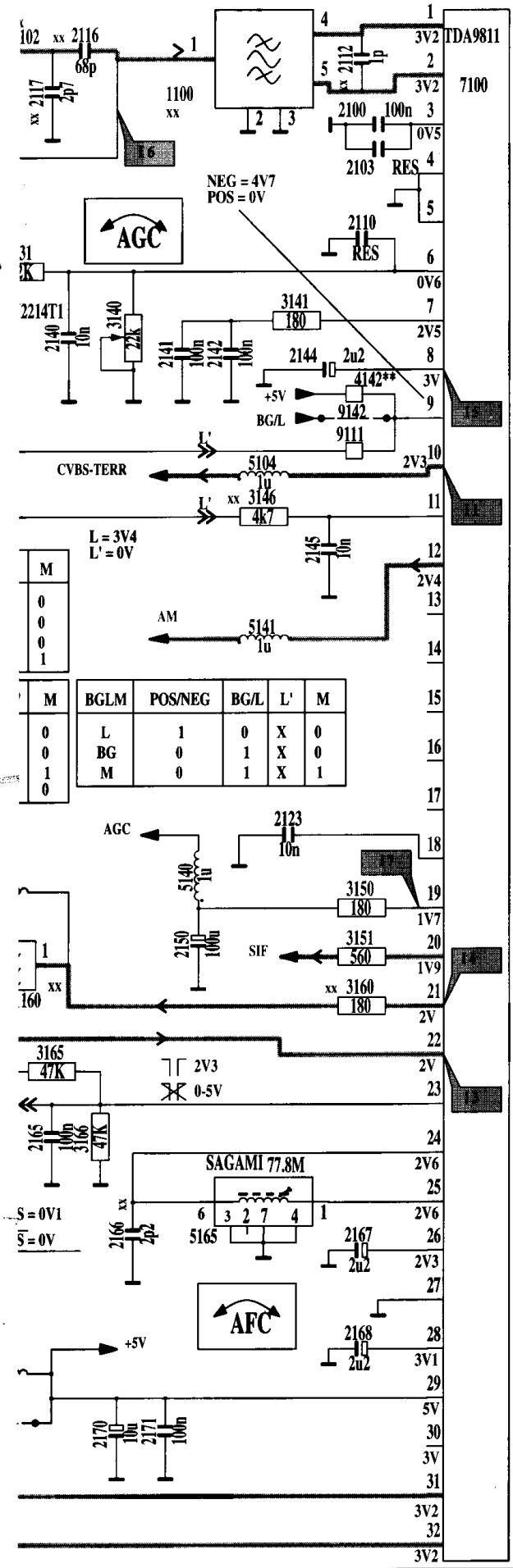
J3.eps
180297

IF module / Zwischenfrequenz-Modul / Module FI

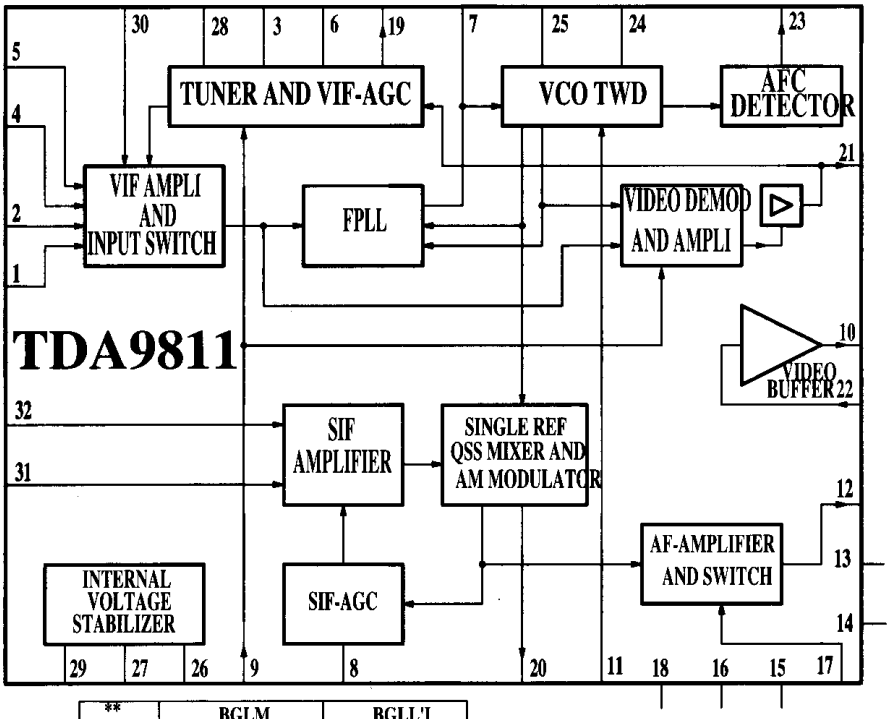


G 9	4112	F 8	5102	A 8	5161	G 7	6110	F 2	7120	G 2	7160	H 7	9111	C10
D 3	4122	F 2	5104	C10	5165	H 9	6111	F 2	7121	H 3	7161	F 7	9142	C10
C 3	4142*	C10	5140	F 9	5170	I 8	6112	G 2	7122	H 3	7190	D 3	9170	I 8
B 2	5100	A 5	5141	D10	6100	A 6	7100	A11	7123	H 2	7191	D 3	N59	A 1
G 6	5101	B 5	5160	F 8	6101	B 5	7110	H 5	7124	B 8	9107	F 6		

IF PANEL



M	BGLM	POS/NEG	BG/L	L'	M
0	L	1	0	X	0
0	BG	0	1	X	0
1	M	0	1	X	1



**	BGLM	BGLL'I
1100	OFWG3956M	OFWG3953M
1102	-	OFWG9354M
1160	TPS5,5MW	TPS6,0MB
1161	TPS4,5MB	TPS5,5MW
2102	68pF	JUMPER
2104	2p7	-
2105	2p7	-
2109	10n	-
2112	-	
2115	JUMPER	330p
2116	-	56p
2117	-	2p2
2120	-	100n
2122	-	100n
3104	150	47
3106	4k7	-
3107	10K	-
3108	2k7	-
3109	1k	-
3121	-	6k8
3124	8k2	6k8
3126	-	2k2
3127	2k2	4k7
3128	2k2	4k7
3129	22k	-
3130	22k	-
3131	22k	-
3146	-	4k7
3160	180	220
4107	JUMPER	-
4108	-	4142
4142	-	-
5101	34,4MC	-
5102	-	40.4MC
6100	BA582	-
6101	BA582	-
6112	-	BA582
7110	MMUN2214T1	-
7120	-	MMUN2214T1
7123	-	MMUN2214T1
7124	MMUN2214T1	-

BGLMDK ; LIKE BGLM EXCEPT:	
1100	OFWG3953M
9111	IN
9142	NOT IN

CHASSIS MD2.2

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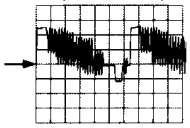
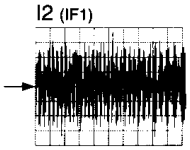
module / Zwi

I1 (CVBS_TERR)



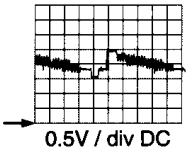
0.5V / div DC
10µs / div

I2 (IF1)



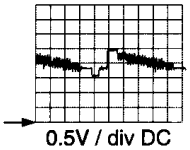
50mV / div DC
50µs / div

I3



0.5V / div DC
10µs / div

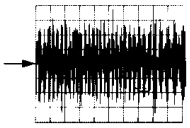
I4



0.5V / div DC
10µs / div

I5
3V DC

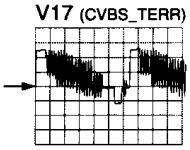
I6



50mV / div DC
50µs / div

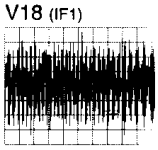
I7 (AGC)
1V9 DC

V17 (CVBS_TERR)



0.5V / div DC
10µs / div

V18 (IF1)



50mV / div DC
50µs / div

→ = 0V

OSC_L.AI
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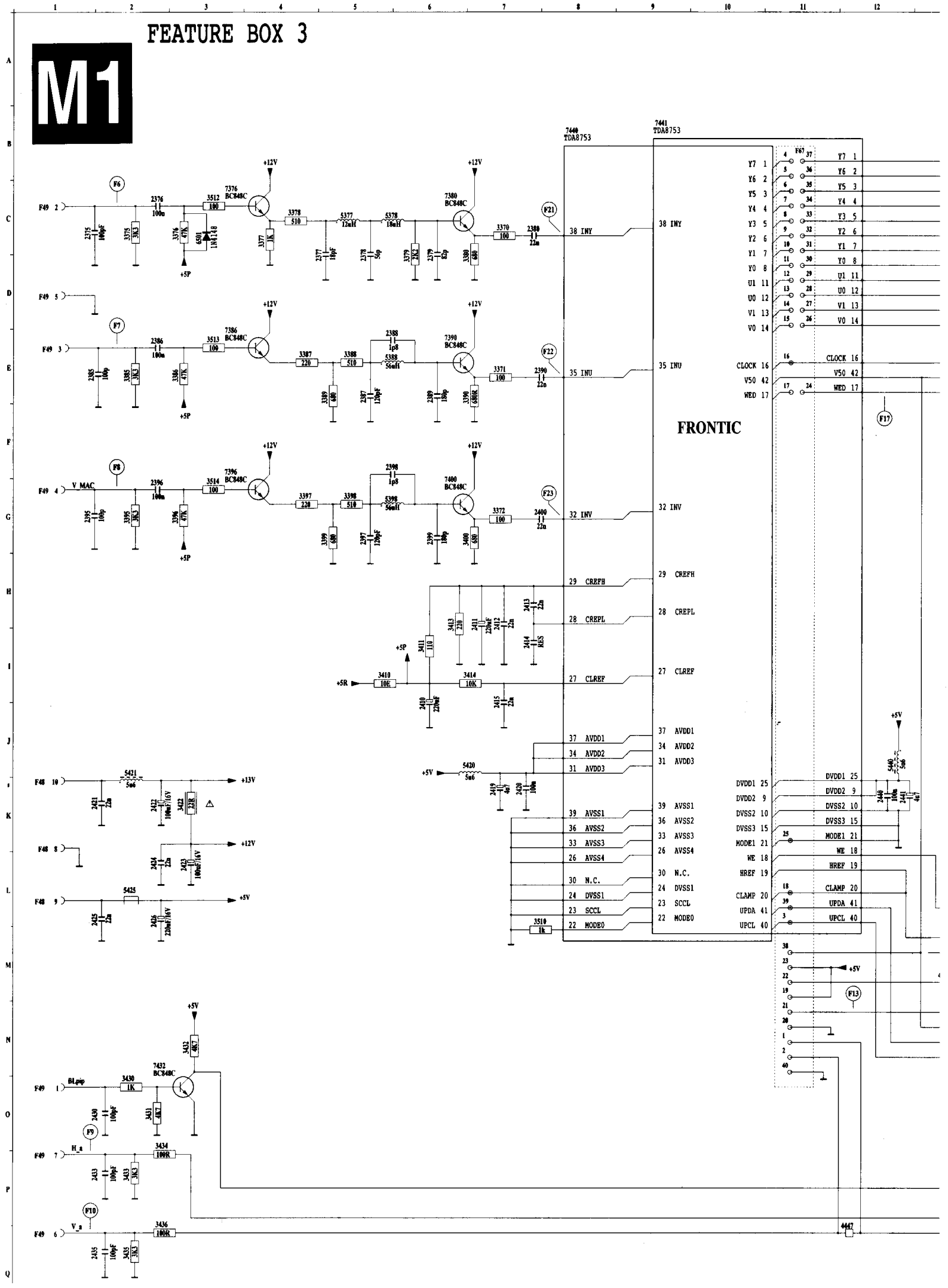
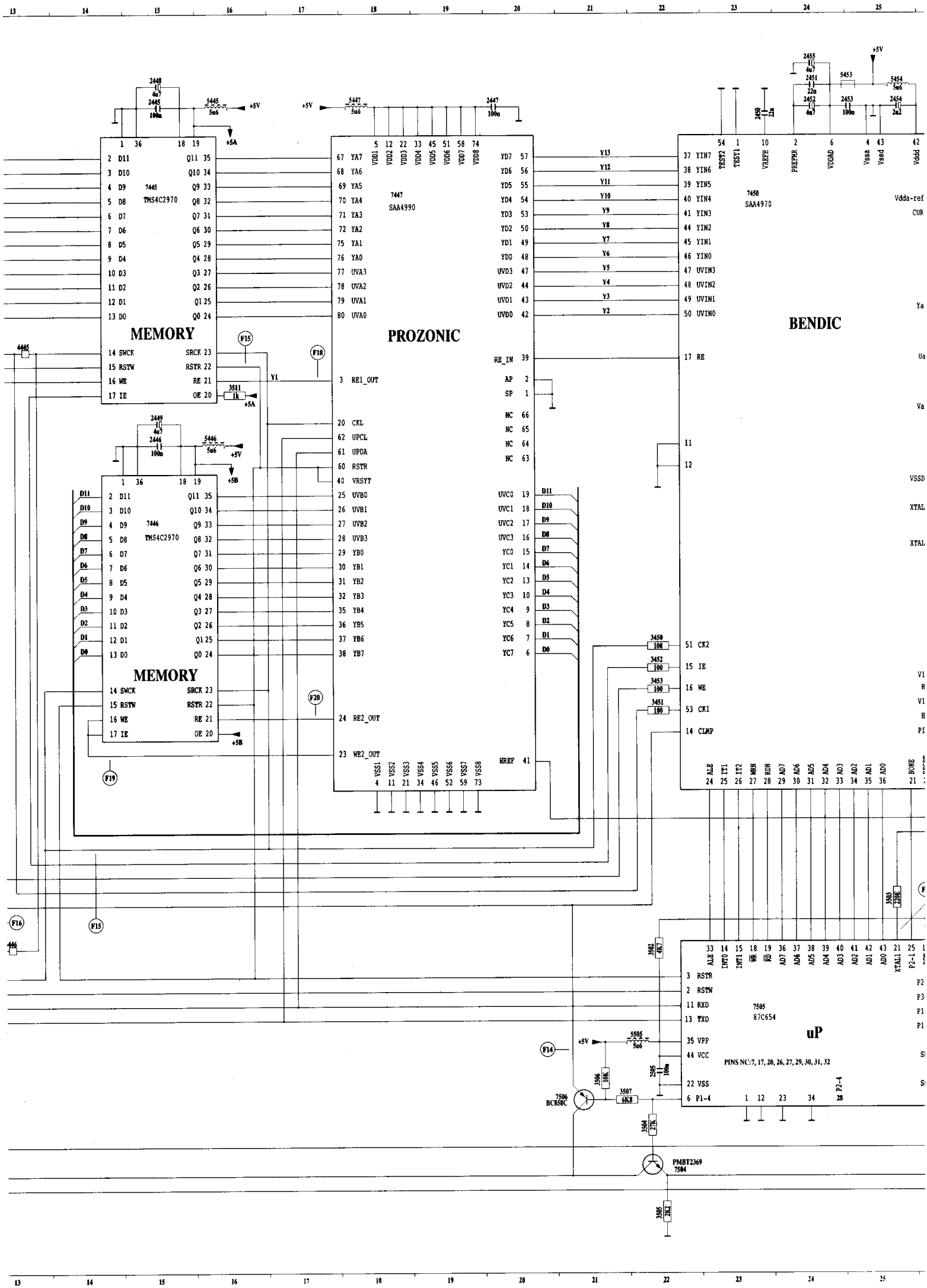
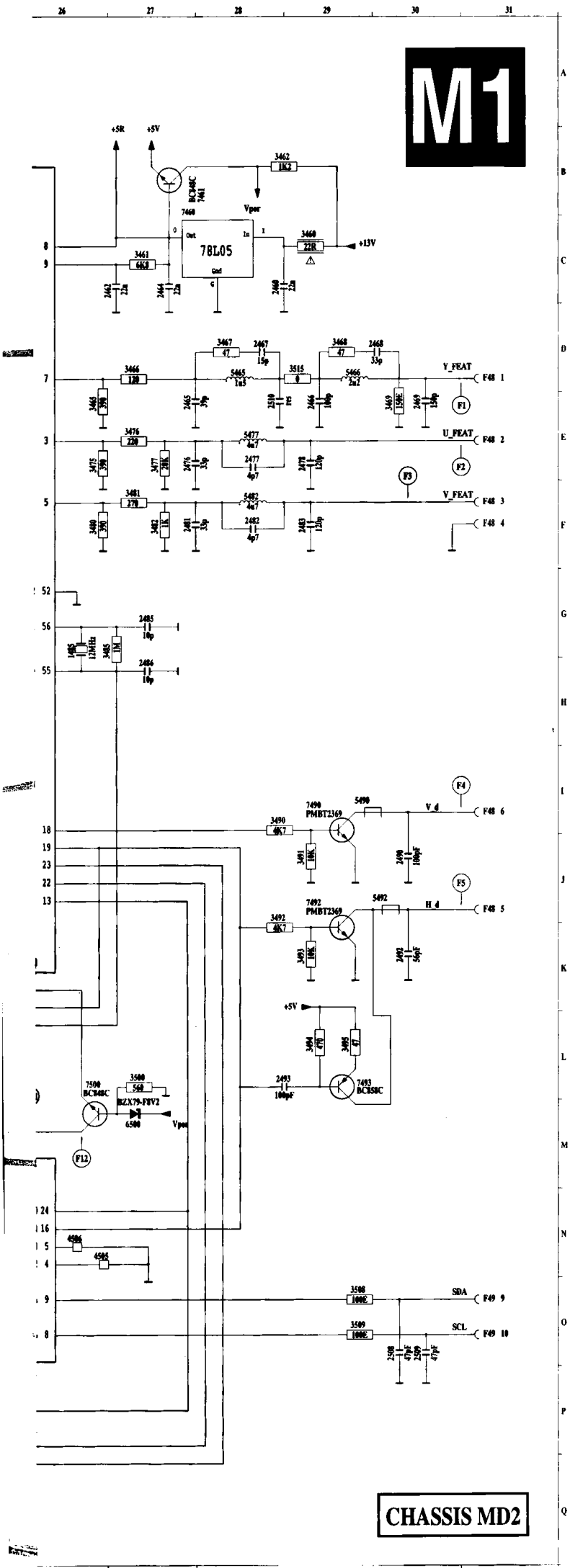
Feature Box (Digital Scan) panel /



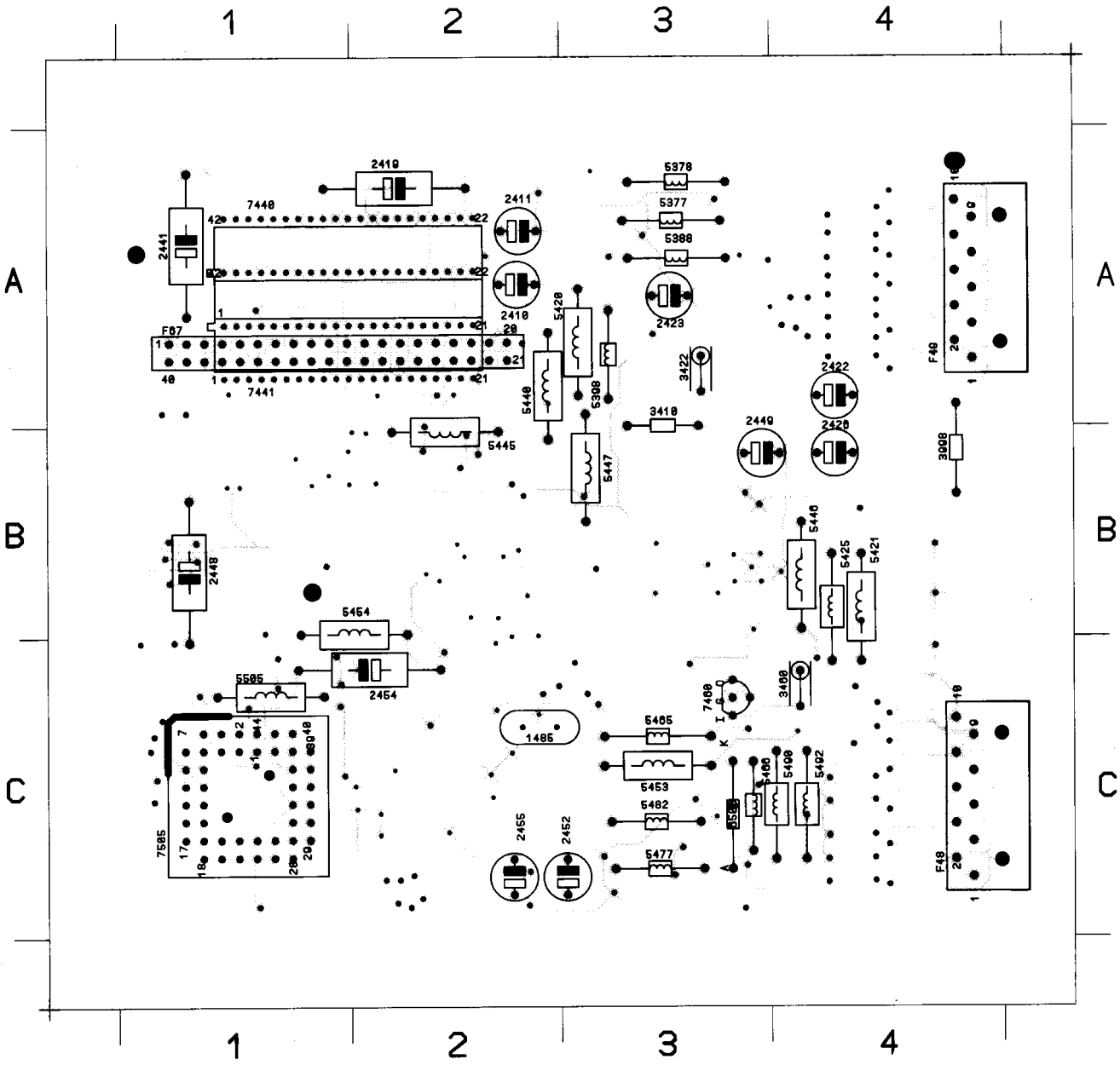

MEMORY
7445
TMS4C2970
MEMORY
7446
TMS4C2970
PROZONIC
7447
SAA4990
BENDIC
7450
SAA4970
uP
7505
87C654
PINS NC:7, 17, 20, 26, 27, 29, 30, 31, 32
7506
BC858C
PMBT2369
7504

Platine Boîtier Numérique (balayage numérique)



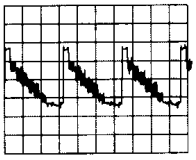
	1485	G26	7450	C23
	2375	C 1	7460	B27
	2376	C 2	7461	B28
	2377	C 5	7490	I29
	2378	C 5	7492	J29
	2379	C 6	7493	L29
A	2380	C 7	7500	L26
	2385	E 1	7504	P22
	2386	E 2	7505	N23
	2387	E 5	7506	O21
	2388	E 6	F48	O31
	2389	E 6	F48	R31
	2390	E 8	F48	F31
	2395	G 1	F48	F31
	2396	G 2	F48	J31
	2397	G 5	F48	I31
	2398	F 6	F48	K 1
	2399	G 6	F48	L 1
B	2400	G 8	F48	K 1
	2410	I 6	F49	O 1
	2411	H 7	F49	C 1
	2412	H 7	F49	E 1
	2413	H 7	F49	G 1
	2414	I 7	F49	D 1
	2415	L 7	F49	Q 1
	2419	K 7	F49	P 1
	2420	K 7	F49	O31
	2421	K 2	F49	O31
	2422	K 2	F67	B11
C	2423	L 1		
	2424	L 2		
	2425	L 2		
	2426	L 2		
	2430	O 2		
	2433	P 2		
	2435	Q 2		
	2440	K12		
	2441	K12		
	2445	A15		
D	2446	F15		
	2447	A20		
	2448	A15		
	2449	F15		
	2450	B23		
	2451	A24		
	2452	A24		
	2453	A25		
	2454	A25		
	2455	A24		
	2460	C28		
E	2462	C27		
	2464	C27		
	2465	E27		
	2466	E29		
	2467	D28		
	2468	D30		
	2469	E30		
	2476	E27		
	2477	E28		
	2478	E29		
	2481	F27		
F	2482	F28		
	2483	F29		
	2485	G27		
	2486	H27		
	2490	J30		
	2492	K30		
	2493	L29		
	2505	O22		
	2508	O30		
	2509	O30		
G	2510	E28		
	3370	C 7		
	3371	E 7		
	3372	G 7		
	3375	C 2		
	3376	C 3		
	3377	C 4		
	3378	C 4		
	3379	C 6		
	3380	C 7		
	3385	E 2		
H	3386	E 3		
	3387	E 4		
	3388	E 5		
	3389	E 5		
	3390	E 7		
	3395	G 2		
	3396	G 3		
	3397	G 4		
	3398	G 5		
	3399	G 5		
	3400	G 7		
I	3410	I 5		
	3411	I 6		
	3413	H 6		
	3414	I 7		
	3422	K 3		
	3430	O 2		
	3431	O 2		
	3432	N 3		
	3433	P 2		
	3434	O 2		
	3435	Q 2		
J	3436	Q 2		
	3450	I22		
	3451	J22		
	3452	I22		
	3453	J22		
	3460	C29		
	3461	C27		
	3462	B29		
	3465	E26		
	3466	D27		
K	3467	D28		
	3468	D29		
	3469	E30		
	3475	E26		
	3476	E27		
	3477	E27		
	3480	F26		
	3481	F27		
	3482	F27		
	3485	G27		
	3490	I28		
L	3491	I29		
	3492	J28		
	3493	K29		
	3494	L29		
	3495	L29		
	3500	L27		
	3502	M22		
	3503	M25		
	3504	P22		
	3505	Q22		
M	3506	O21		
	3507	O21		
	3508	O29		
	3509	O29		
	3510	L 8		
	3511	E16		
	3512	C 3		
	3513	E 3		
	3514	G 3		
	3515	D29		
	3998	M 5		
N	3999	N 5		
	4445	E13		
	4446	M13		
	4447	Q12		
	4505	N26		
	4506	N26		
	5377	C 5		
	5378	C 6		
	5388	E 6		
	5398	G 6		
	5420	J 7		
O	5421	J 2		
	5425	L 2		
	5440	J12		
	5445	A16		
	5446	F16		
	5447	A18		
	5453	A25		
	5454	A25		
	5465	D28		
	5466	D29		
	5477	E28		
P	5482	F28		
	5490	I29		
	5492	J30		
	5505	N22		
	6500	M27		
	6501	C 3		
	7376	C 3		
	7380	C 6		
	7386	E 3		
	7390	E 6		
	7396	F 3		
	7400	G 6		
Q	7432	N 2		
	7440	B 8		
	7441	B 9		
	7445	C15		
	7446	G15		
	7447	C18		

Feature Box (Digital Scan) panel /



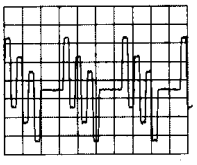
1485 C 2	2419 A 1	2426 B 4	2449 B 3	2455 C 2	3460 C 4	5378 A 3	5420 A 3	5440 B 2	5447 A 3	5465 C 3	5482 C 3	5505 C 1	7441 A 1	F48 C 4
2410 A 2	2422 A 4	2441 A 1	2452 C 3	3410 A 3	3998 B 4	5388 A 3	5421 C 4	5445 B 2	5453 C 3	5466 C 3	5490 C 4	6500 C 3	7460 C 3	F49 A 4
2411 A 2	2423 A 3	2448 B 1	2454 C 2	3422 A 3	5377 A 3	5398 A 3	5425 C 4	5446 B 4	5454 B 1	5477 C 3	5492 C 4	7440 A 1	7505 C 1	F07 A 1

F1



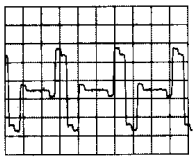
100mV/div
10µs/div

F2



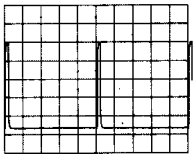
200mV/div
10µs/div

F3



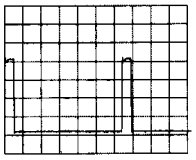
200mV/div
10µs/div

F4



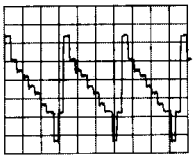
1V/div
2ms/div

F5



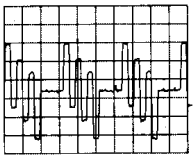
1V/div
5µs/div

F6



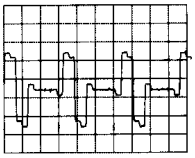
200mV/div
20µs/div

F7



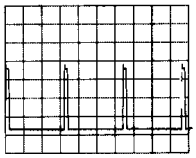
200mV/div
20µs/div

F8



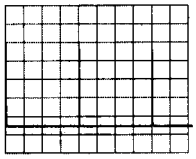
200mV/div
20µs/div

F9



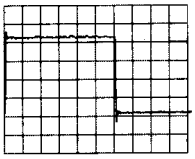
1V/div
20µs/div

F10



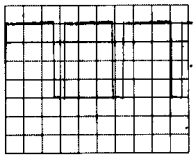
1V/div
5ms/div

F16



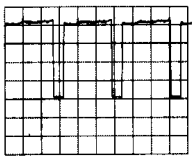
1V/div
0.5µs/div

F17



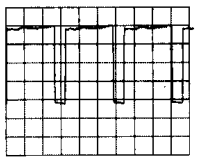
1V/div
20µs/div

F18



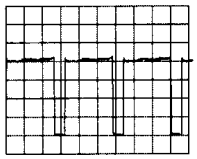
1V/div
10µs/div

F19



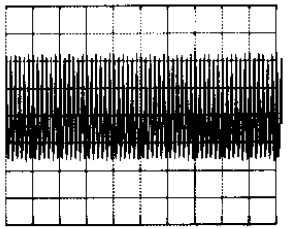
1V/div
10µs/div

F20



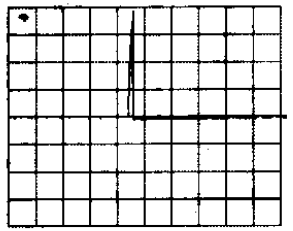
1V/div
10µs/div

F11



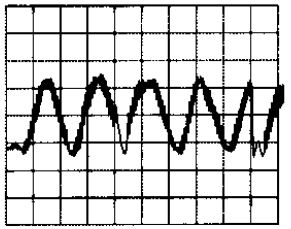
1V/div
0.5µs/div

F12



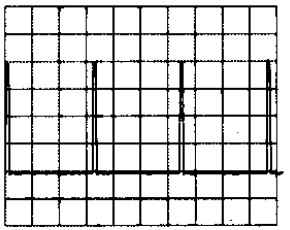
1V/div
50ms/div

F13



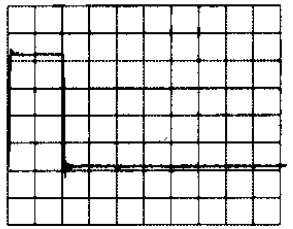
500V/div
50ns/div

F14



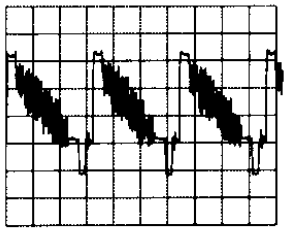
1V/div
20µs/div

F15



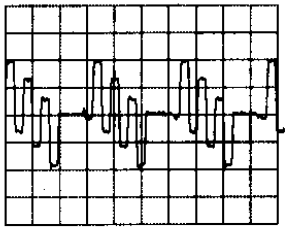
1V/div
0.5µs/div

F21



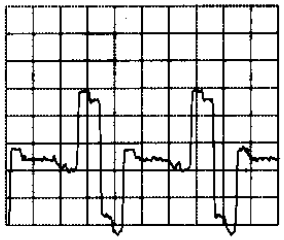
200mV/div
20µs/div

F22



200mV/div
20µs/div

F23



200mV/div
20µs/div

PCS 91 167