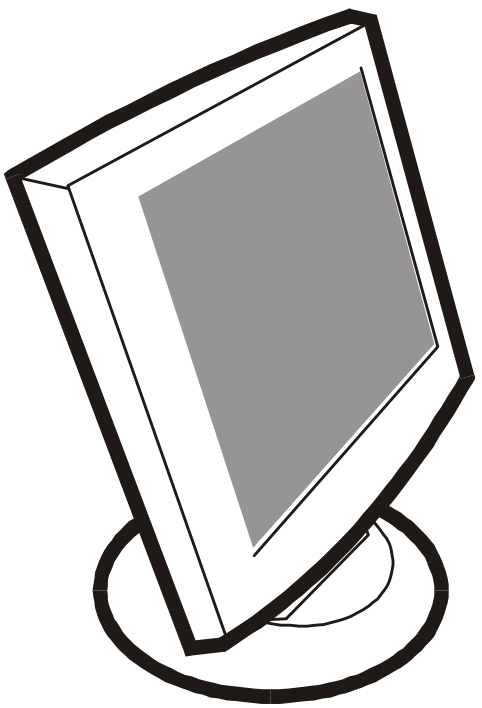
SERVICE MANUAL

TF1560GH C383 S383FA-V151



FUJITSU COMPUTERS
SIEMENS

P/N：41A50-137

5. CIRCUIT-DESCRIPTION

5-1 THE DIFFERENT between LG-Panel & Samsung-Panel & CPT-Panel & Hannstar- Panel in ELECTRICAL Charateristic

LG-Panel
1. Two CCFL (Cold Cathode Fluorescent Tube)
2. Single Pixel, 6 bit color (262144 colors)
3. Panel Vdd = 3.3V (in JP202 select 3.3V)

Samsung-Panel
1. Four CCFL (Cold Cathode Fluorescent Tube)
2. Double Pixel, 6 bit color (262144 colors)
3. Panel Vdd = 5V (in JP201 select 5V)

Chung-Hwa Panel
1. Two CCFL (Cold Cathode Flourescent Tube)
2. Double Pixel, 8 bit color (16.7 Million colors)
3. Panel Vdd = 5V (in JP201 select 5V)

Hannstar Panel
1. Two CCFL (Cold Cathode Flourescent Tube)
2. Double Pixel, 6 bit color (262144 colors)
3. Panel Vdd = 3.3V (in JP202 select 3.3V)

5-2 SPECIAL FUNCTION with PRESS-KEY

press ENTER-key 2 seconds, at POWER-ON: set to FACTORY-mode, when we want to adjust white-balance with rs232-port or view Power-on-timer. In this mode, OSD-screen will locate in left top of screen.

Press POWER-key off-on : CANCEL above function(quit from factory mode) and set to user-mode.

Press both Left & Right key and switching on-off key : Enable/ Disable OSD-LOCK function

OSD-INDEX EXPLANATION

1. CABLE NOT CONNECTED : Signal-cable not connected.
2. INPUT NOT SUPPORT :
   a. INPUT frequency out of range : H > 62kHz, v > 75Hz or H < 28kHz, v < 55Hz
   b. INPUT frequency out of VESA-spec. (out of tolerance too far)
3. UNSUPPORT mode, try different Video-card Setting :
   Input frequency out of tolerance, but still can catch-up by our system (if this message show, that means, this is new-user mode, AUTO-CONFIG will disable)

5-3 SIMPLE-INTRODUCTION about LM500 chipset

1. GMZAN1 (Genesis all-in-one solution for ADC, OSD, scalar and interpolation) :
   USE for computer graphics images to convert analog RGB data to digital data for interpolation process, zooming, OSD font & overlay and generate drive-timing for LCD-PANEL,

2. M6759 (ALI- MCU, type 8052 series with 64k Rom-size and 512 byte ram) :
   Use for calculate frequency, pixel-dot , detect change mode, rs232-communication, power-consumption control, OSD-index warning…etc.

3. 24LC21 (MicroChip IC) :
   EePROM type, 1K ROM-SIZE, for saving DDC-CONTENT.

4. 24C04 (ATMEL IC) :
   EePROM type, 4K ROM-SIZE, for saving AUTO-config data, White-balance data, and Power-key status and power on –counter data.

5. LM2569S(NS brand swintching regulator 12V to 5V with 3A load current) :

6. AIC 1084-33CM (AIC brand linear regulator 5V to 3.3V)

MODULE-TPYE COMPONENT :

1. ADAPTER : CONVERSION-module to convert AC 110V-240V to 12VDC, with 3.5 AMP

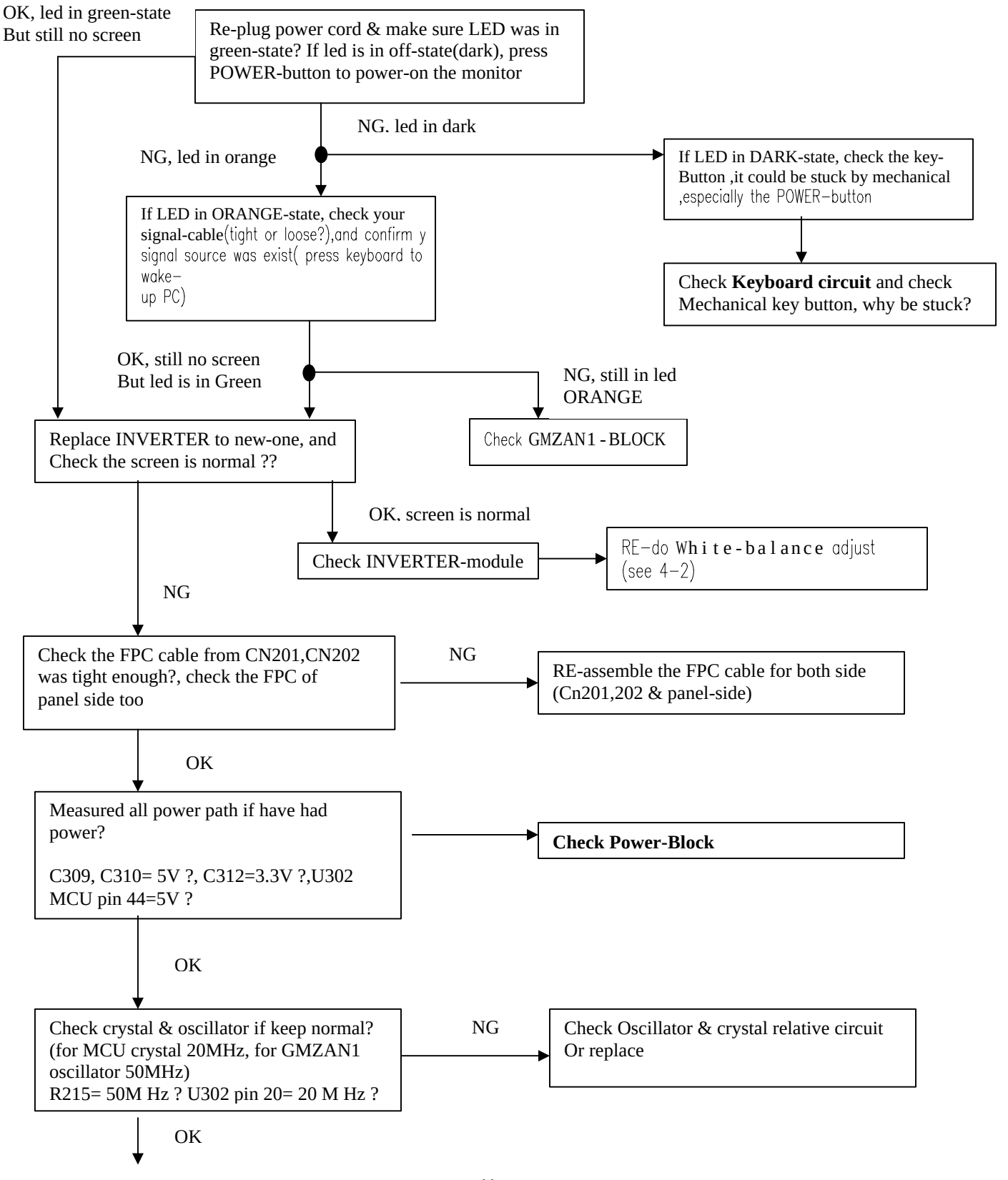
2. INVERTER : CONVERSION-module to convert DC 12V to High-Voltage around 1600V, with frequency 30K-50Khz, 7mA-9mA

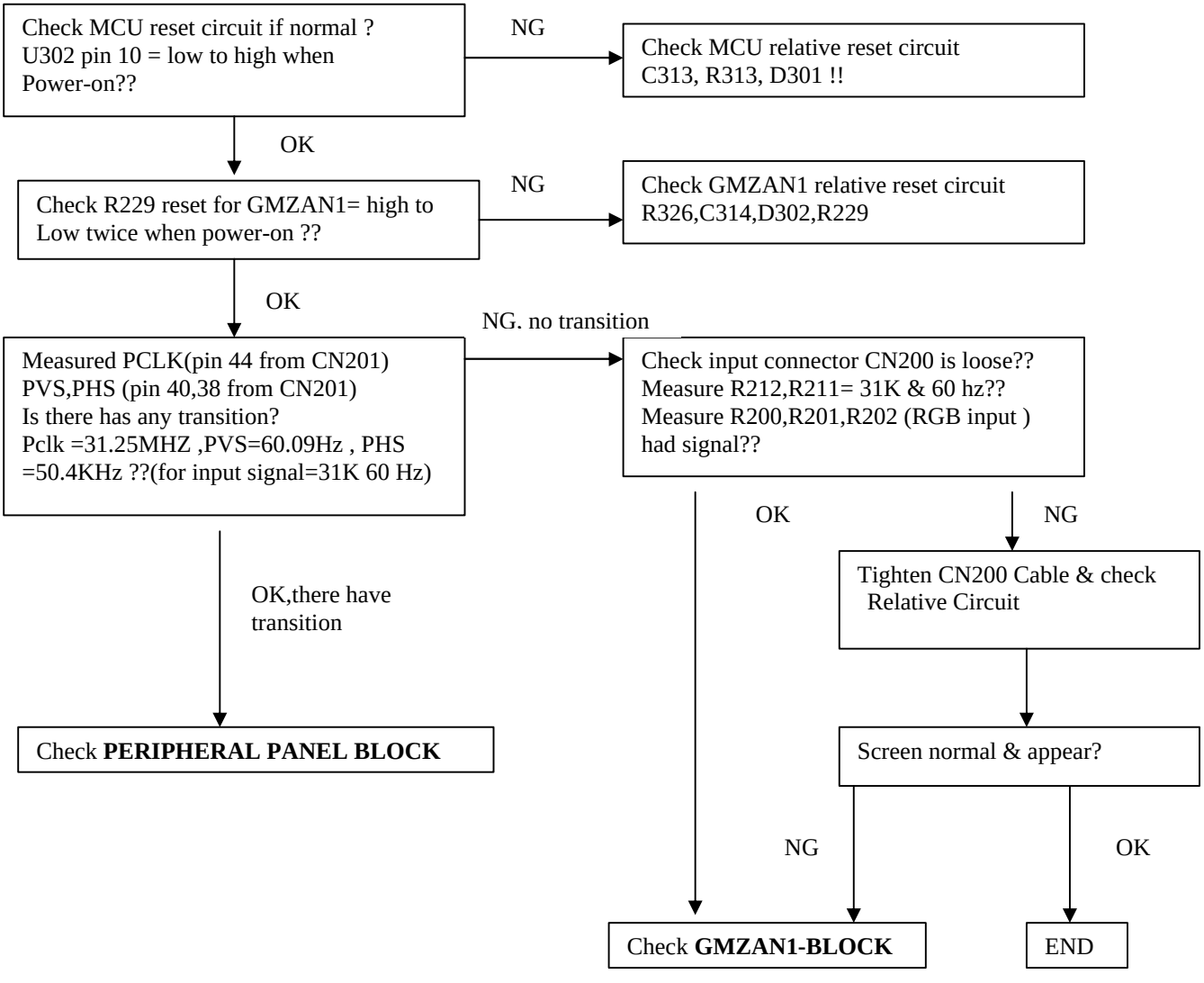
6. Trouble-Shooting

****Use the PC Win 98/95 white pattern, with some icon on it, and Change the Resolution to 640x480 60 Hz / 31 KHz**

****NOTICE : This system free-running freq. is 48 KHz / 60 Hz, so you better use another frequency to do trouble shooting(ex:31kHz 60Hz) this trouble shooting is proceed with 640x480 @60Hz 31Khz**

I. NO SCREEN APPEAR




Check MCU reset circuit if normal ?
U302 pin 10 = low to high when Power-on??
NG
Check MCU relative reset circuit
C313, R313, D301 !!
OK
Check R229 reset for GMZAN1= high to Low twice when power-on ??
NG
Check GMZAN1 relative reset circuit
R326,C314,D302,R229
OK
NG. no transition
Measured PCLK(pin 44 from CN201)
PVS,PHS (pin 40,38 from CN201)
Is there has any transition?
Pclk =31.25MHZ ,PVS=60.09Hz , PHS =50.4KHz ??(for input signal=31K 60 Hz)
Check input connector CN200 is loose??
Measure R212,R211= 31K & 60 hz??
Measure R200,R201,R202 (RGB input) had signal??
OK
NG
Tighten CN200 Cable & check Relative Circuit
OK,there have transition
Check PERIPHERAL PANEL BLOCK
Screen normal & appear?
NG
OK
Check GMZAN1-BLOCK
END

PERIPHERAL PANEL BLOCK

Note: “Panel vdd “ and “backlight on-off ” can be direct control by :

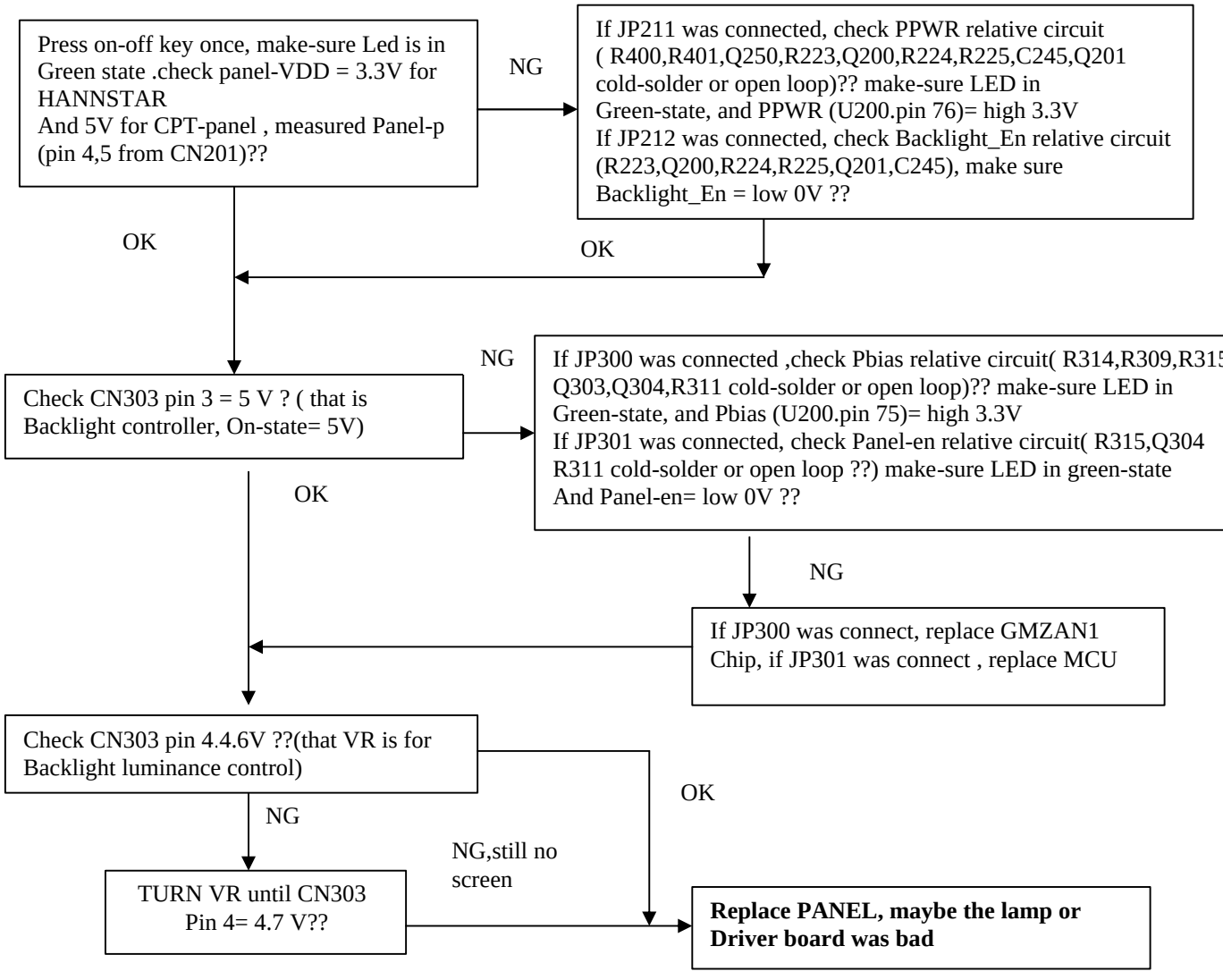
GMZAN1 or MCU

Some panel can direct control by GMZAN1 ,if the relative timing between panel-vdd and backlight on-off is short (under 80 ms) , otherwise, will be control by MCU

If J211 be connected, that means Panel-VDD control was by GMZAN1 ,otherwise by MCU(JP212)

If J300 be connected, that means Backlight control was by GMZAN1 ,otherwise by MCU (JP301)

BUT Hannstar panel & CPT panel still control by J211 & J300

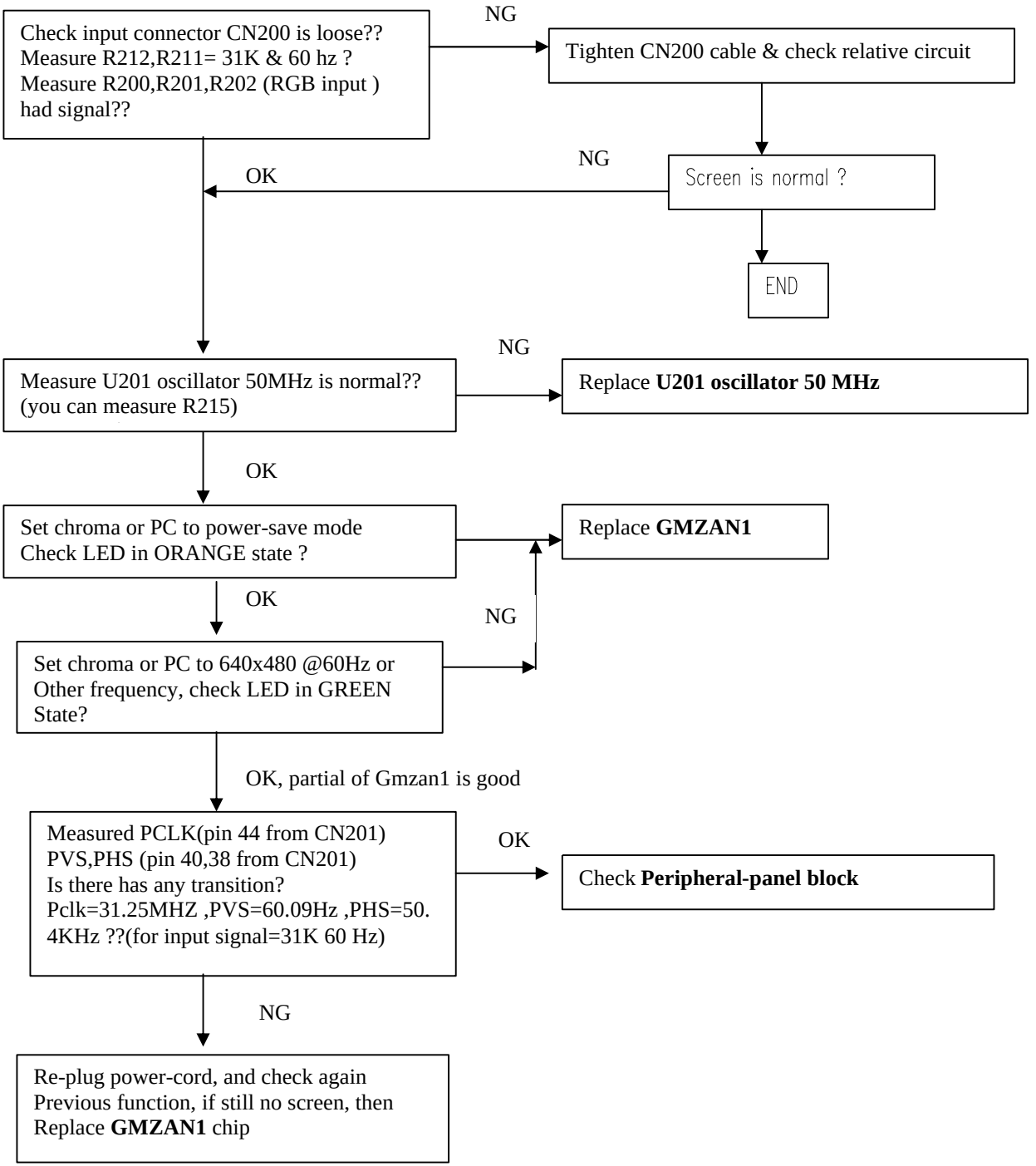


FOR HANNSTAR-PANEL , there is the relative timing between input resolution to output timing for panel (output timing from GMZAN1 chip) as follow :

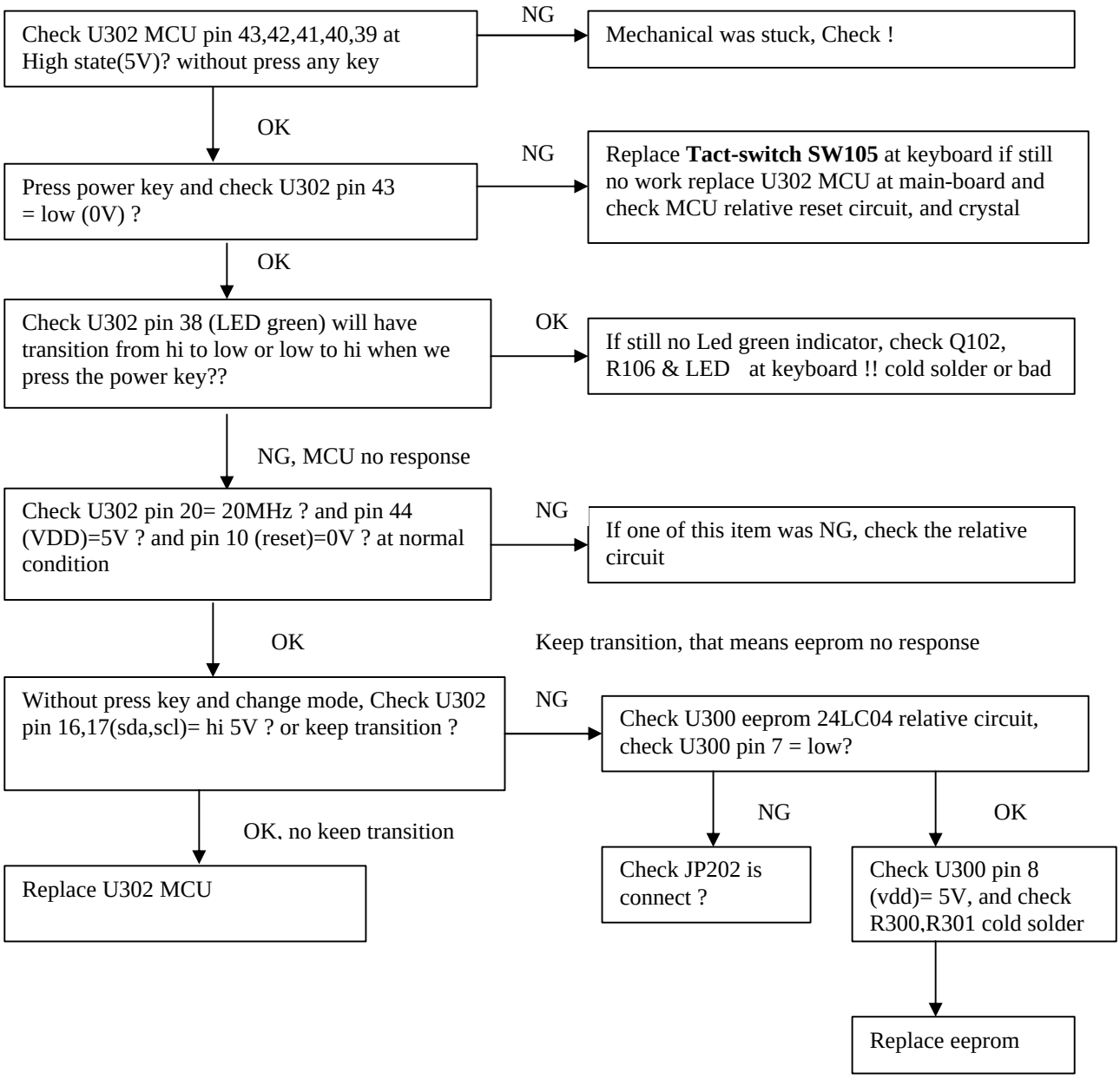
RESOLUTION(from PC or chroma)	PCLK(U200.44)	PHS (U200.74)	PVS (U200.73)
640X480 @60 Hz	31.25MHz	50.4 KHz	60.09 Hz
640X480 @70 Hz	35.56MHz	55.93KHz	69.83 Hz
640X480 @72 Hz	36.76MHz	57.64KHz	71.94 Hz
640X480 @75 Hz	37.71MHz	60.12KHz	74.96 Hz
800X600 @60 Hz	28.65MHz	48.45KHz	60.39 Hz
800X600 @70 Hz	32.94MHz	56.05KHz	70.03 Hz
800X600 @72 Hz	34.25MHz	57.61KHz	72.04 Hz
800X600 @75 Hz	35.71MHz	60.10KHz	75.08 Hz
1024x768@60 Hz	28.57MHz	48.36KHz	60.09 Hz
1024x768@70 Hz	32.77MHz	56.05KHz	70.03 Hz
1024x768 @72 Hz	33.97MHz	57.60KHz	71.84 Hz
1024x768@75 Hz	35.41MHz	60.24KHz	74.96 Hz

GMZAN1 BLOCK check

Note : set the input signal (PC or CHROMA) to 640x480 31k 60 hz



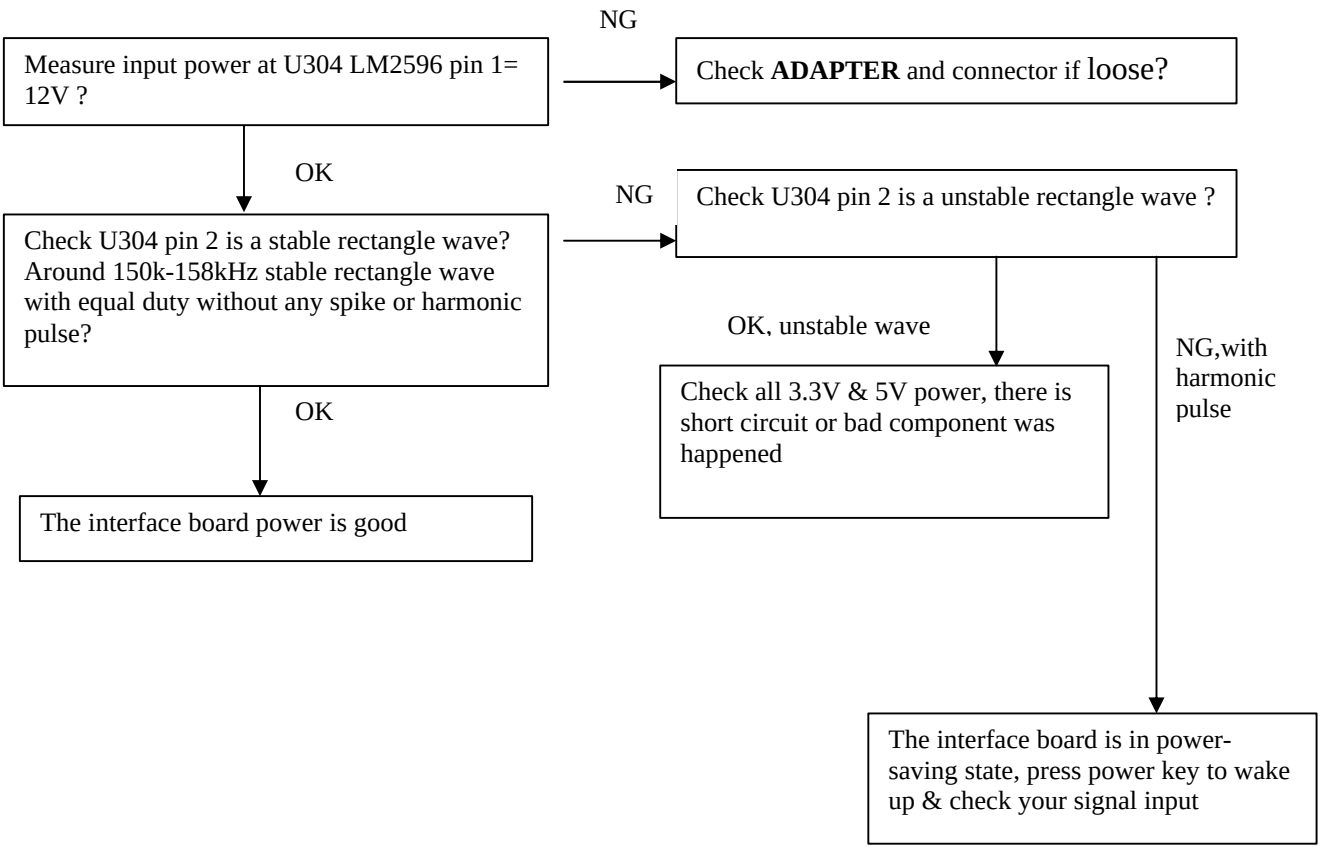
KEYBOARD BLOCK check



POWER-BLOCK check

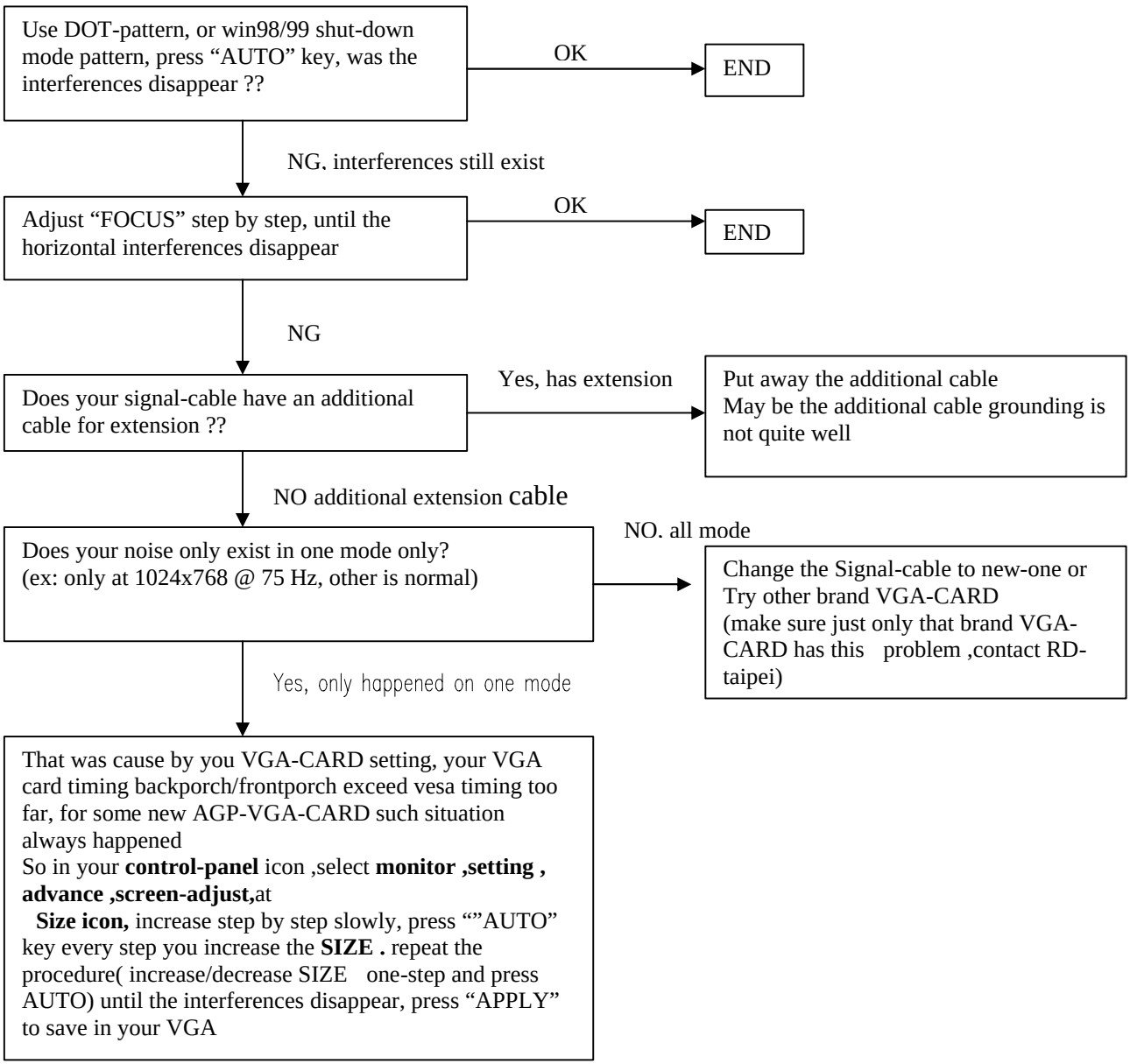
**Note : the waving of U304 pin 2 can determined the power situation

1. stable rectangle wave with equal duty, freq around 150K-158KHz
   that means all power of this interface board is in normal operation
   ,all status of 5V & 3.3V is normal working
2. unstable rectangle wave without same duty, that means ABNORMAL operation was happened
   check 3.3V or 5V ,short-circuit or bad component
3. rectangle wave with large spike & harmonic pulse on front side of rectangle wave, that means all 3.3v is no load, **Gmzan1** was shut-down, and only **MCU** still working ,the monitor is in power saving state



II.ALL SCREEN HAS INTERFERENCES OR NOISE, CAN'T BE FIXED BY AUTO KEY

**** NOTE:** There is so many kind of interferences, 1). One is cause by some VGA-CARD that not meet VESA spec or power grounding too bad that influence our circuit
2).other is cause by external interferences, move the monitor far from electronic equipment.(rarely happened)



III. DOS MODE has jitter

NOTE :the rule of doing AUTO-CONFIGURATION : must be a full-size screen, if the screen not full , the auto-configuration will fail. So in dos mode ,just set your "CLOCK" in OSD-MENU to zero or use some full screen edit file (ex: PE2, HE) and press "AUTO"

I? . THERE WAS SNOW PHENOMENA or BRIGHT NOISE ON THE SCREEN

When use pattern 32 Gray-scale / or 16 Gray scale, there is a **snow phenomena on the screen (like a noise spread** inside) that means some output bit to panel was bad, may be cause by FPC loose, or bead-array cold-solder

There were some panel (ex :LG),also have this phenomena too, the noise will reduce or increase depend on the contrast/brightness value, this kind of problem was cause by Panel-driver-board it self, we can't fix it ,the only way to do was find the best-point of brightness/contrast, that the noise is more light

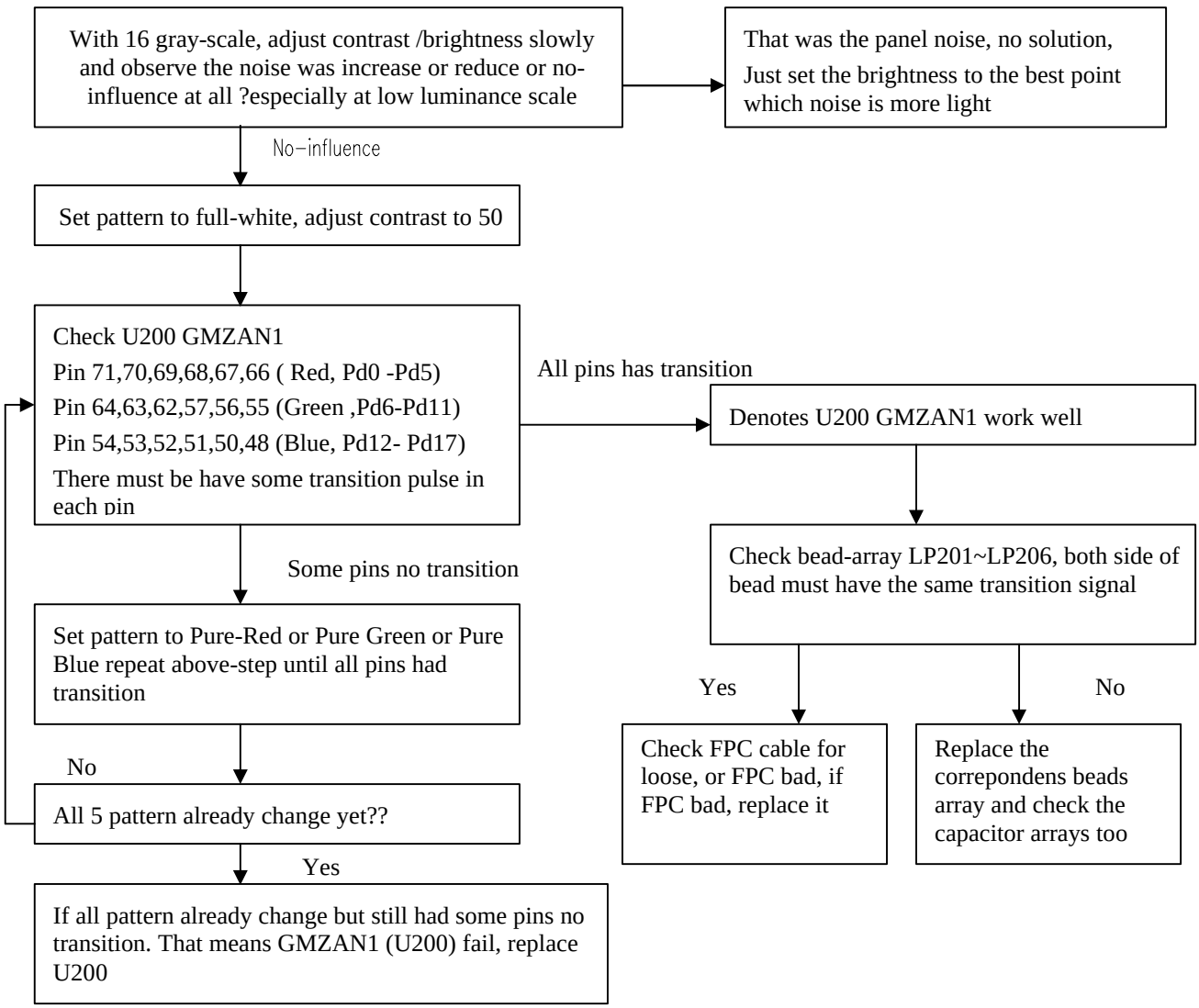
Use following pattern :

1. pure-white	2. Pure Red	3. Pure Green
4. Pure Blue	5. Pure White	6. Character

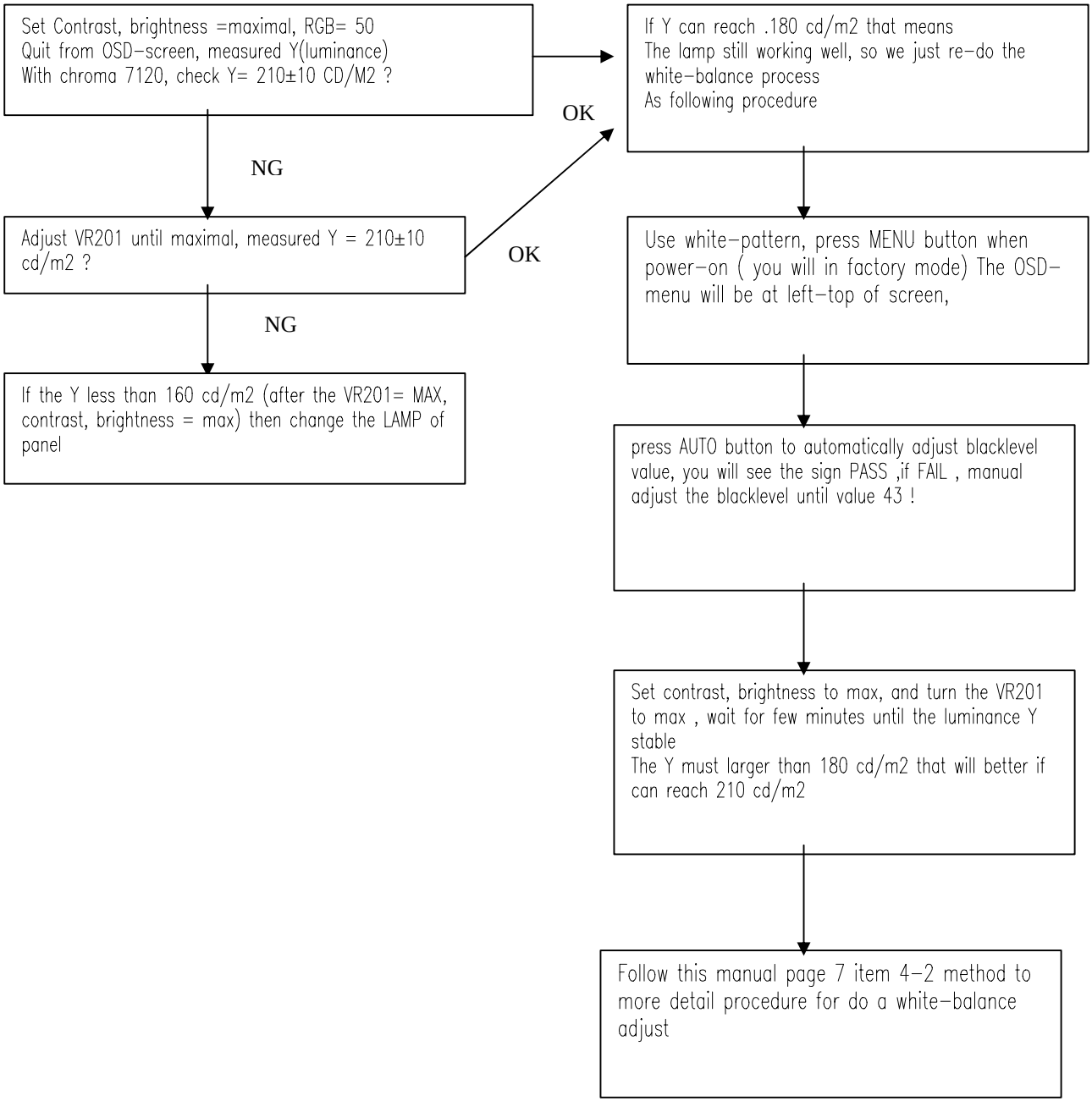
repeat measure GMZAN1 (U200) all output pins must have some transition pulse, but notice

1. For LG panel and HANNSTAR panel , only 6 bit has output, (PD0~ PD17 , PD36 ~ PD41) the corresponding beads was LP201 ~ LP206
2. For Chung-hwa panel or other's 8 bit panel, all output are available (PD0-PD47), the corresponding beads was LP201-LP212

Ex : HANNSTAR Panel 6 bits



V. THE PANEL LUMINANCE WAS DOWN



GMZAN1

The gmZAN1device utilizes Genesis' patented third-generation Advanced Image Magnification technology as well as a proven integrated ADC/PLL to provide excellent image quality within a cost effective SVGA/XGA LCD monitor solution.
As a pin-compatible replacement for the gmB120, the gmZAN1 incorporates all of the gmB120 features plus many enhanced features; including 10-bit gamma correction, Adaptive Contrast Enhancement (ACE) filtering, Sync On Green (SOG), and an enhanced OSD.

1.1 Features

- Fully integrated 135MHz 8-bit triple-ADC, PLL, and pre-amplifier
- GmZ2 scaling algorithm featuring new Adaptive Contrast Enhancement (ACE)
- On-chip programmable OSD engine
- Integrated PLLs
- 10-bit programmable gamma correction
- Host interface with 1 or 4 data bits
- Pin-compatible with gmB120

Integrated Analog Front End

- Integrated 8-bit triple ADC
- Up to 135MHz sampling rates
- No additional components needed
- All color depths up to 24-bits/pixel are supported

High-Quality Advanced Scaling

- Fully programmable zoom
- Independent horizontal / vertical zoom
- Enhanced and adaptive scaling algorithm for optimal image quality
- Recovery Mode / Native Mode

Input Format

- Analog RGB up to XGA 85Hz
- Support for Sync On Green (SOG)
- Support for composite sync modes

Output Format

- Support for 8 or 6-bit panels (with high quality dithering)
- One or two pixel output format

Built In High-Speed Clock Generator

- Fully programmable timing parameters
- On-chip PLLs generate clocks for the on-chip ADC and pixel clock from a single reference oscillator

Auto-Configuration / Auto-Detection

- Phase and image positioning
- Input format detection

Operation Modes

- Bypass mode with no filtering
- Multiple zoom modes:
  - With filtering
  - With adaptive (ACE) filtering

Integrated On-Screen Display

- On-chip character RAM and ROM for better customization
- External OSD supported for greater flexibility
- Supports both landscape and portrait fonts
- Many other font capabilities including: blinking, overlay and transparency

1.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 1 : Analog-to-Digital Converter

PIN #	Name	I/O	Description
77	ADC_VDD2		Digital power for ADC encoding logic. Must be bypassed with 0.1uF capacitor to pin 78 (ADC_GND2)
78	ADC_GND2		Digital GND for ADC encoding logic. Must be directly connected to the digital system ground plane.
79	ADC_VDD1		Digital power for ADC clocking circuit. Must by passed with 0.1uF capacitor to pin 80 (ACD_GND1).
80	ADC_GND1		Digital GND for ADC clocking circuit. Must be directly connected to the digital system ground plane.
81	SUB_GNDA		Dedicated pin for substrate guard ring that protects the ADC reference system. Must be directly connected to the analog system ground plane.
82	ADC_GNDA		Analog ground for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Must be directly connected to analog system ground plane.
84	ADC_VDDA		Analog power for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Must be bypassed with 0.1uF capacitor to pin 82 (ADC_GNDA).
83	Reserved		For internal testing purpose only. Do not connect.
85	ADC_BGNDA		Analog ground for the blue channel. Must be directly connected to the analog system ground plane.
88	ADC_BVDDA		Analog power for the blue channel. Must be bypassed with 0.1uF capacitor to pin 85(BGNDA).
86	BLUE-	I	Negative analog input for the Blue channel.
87	BLUE+	I	Positive analog input for the Blue channel.
89	ADC_GGNDA		Analog ground for the green channel. Must be directly connected to the analog system ground plane.
92	ADC_GVDDA		Analog power for the green channel. Must be bypassed with 0.1uF capacitor to pin 89 (ADC_GGNDA).
90	GREEN-	I	Negative analog input for the Green channel.
91	GREEN+	I	Positive analog input for the Green channel.
93	ADC_RGNDA		Analog ground for the red channel. Must be directly connected to the analog system ground plane.
96	ADC_RVDDA		Analog power for the red channel. Must be bypassed with 0.1uF capacitor to pin 93 (ADC_RGNDA).
94	RED-	I	Negative analog input for the Red channel.
95	RED+	I	Positive analog input for the Red channel.

Table 2 : Host Interface (HIF) / External On-Screen Display

PIN #	Name	I/O	Description
98	HFS	I	Host Frame Sync. Frames the packet on the serial channel.
103	HCLK	I	Clock signal input for the 3-wire serial communication.
99	HDATA	I/O	Data signal for the 3-wire serial communication.
100	RESETn	I	Resets the gmZAN1 chip to a known state when low.
101	IRQ	O	Interrupt request output.
115	OSD-HREF	O	HSYNC output for an external OSD controller chip.
116	OSD-VREF	O	VSYNC output for an external OSD controller chip.
117	OSD-Clk	O	Clock output for an external OSD controller chip.
118	OSD-Data0	I	Data input 0 from an external OSD controller chip.
119	OSD-Data1	I	Data input 1 from an external OSD controller chip.
120	OSD-Data2	I	Data input 2 from an external OSD controller chip.
121	OSD-Data3	I	Data input 3 from an external OSD controller chip.
122	OSD-FSW	I	External OSD window display enable. Displays data from external OSD controller when high.
123	MFB11	I/O	Multi-Function Bus 11. One of twelve multi-function signals MFB[11:0].
124	MFB10	I/O	Multi-Function Bus 10. One of twelve multi-function signals MFB[11:0].
102	MFB9	I/O	Multi-Function Bus 9. One of twelve multi-function signals MFB[11:0]. Also used as HDATA3 in a 4-bit host interface configuration.
104	MFB8	I/O	Multi-Function Bus 8. One of twelve multi-function signals MFB[11:0]. Also used as HDATA2 in a 4-bit host interface configuration.
105	MFB7	I/O	Multi-Function Bus 7. One of twelve multi-function signals MFB[11:0]. Also used as HDATA1 in a 4-bit host interface configuration.
106	MFB6	I/O	Multi-Function Bus 6. One of twelve multi-function signals MFB[11:0]. Internally pulled up. When externally pulled down (sampled at reset) the host interface is configured for 4 bits wide. In this configuration, MFB9:7 are used as HDATA 3:1.
107	MFB5	I/O	Multi-Function Bus 5 One of twelve multi-function signals MFB[11:0]. Internally pulled up. When externally pulled down (sampled at reset) the chip uses an external crystal resonator across pins 141 and 142, instead of an oscillator.
109	MFB4	I/O	Multi-Function Bus 4. One of twelve multi-function signals MFB[11:0].
110	MFB3	I/O	Multi-Function Bus 3. One of twelve multi-function signals MFB[11:0].
111	FMB2	I/O	Multi-Function Bus 2. One of twelve multi-function signals MFB[11:0].
112	MFB1	I/O	Multi-Function Bus 1. One of twelve multi-function signals MFB[11:0].
113	MFB0	I/O	Multi-Function Bus 0. One of twelve multi-function signals MFB[11:0].

Table 3 : Clock Recovery / Time Base Conversion

PIN #	Name	I/O	Description
125	DVDD		Digital power for Destination DDS (direct digital synthesizer). Must be bypassed with a 0.1uF capacitor to digital ground plane.
127	DAC_DGNDA		Analog ground for Destination DDS DAC. Must be directly connected to the analog system ground plane.
128	DAC_DVDDA		Analog power for Destination DDS DAC. Must be bypassed with a 0.1uF capacitor to pin 127 (DAC_DGNDA).
129	PLL_DVDDA		Analog power for the Destination DDS PLL. Must be bypassed with a 0.1uF capacitor to pin 131 (PLL_DGNDA).
130	Reserved		For testing purposes only. Do not connect.
131	PLL_DGNDA		Analog ground for the Destination DDS PLL. Must be directly connected to the analog system ground plane.
132	SUB_DGNDA		Dedicated pin for the substrate guard ring that protects the Destination DDS. Must be directly connected to the analog system ground plane.
133	SUB_SGNDA		Dedicated pin for the substrate guard ring that protects the Source DDS. Must be directly connected to the analog system ground plane.
134	PLL_SGNDA		Analog ground for the Source DDS PLL. Must be directly connected to the analog system ground.
135	Reserved		For testing purposes only. Do not connect.
136	PLL_SVDDA		Analog power for the Source DDS DAC. Must be bypassed with a 0.1uF capacitor to pin 134 (PLL_SGNDA)
137	DAC_SVDDA		Analog power for the Source DDS DAC. Must be by passed with a 0.1uF capacitor to pin 138 (DAC_SGNDA)
138	DAC_SGNDA		Analog power for the Source DDS DAC. Must be directly connected to the analog system ground.
139	SVDD		Digital power for the Source DDS. Must be bypassed with a 0.1uF capacitor to digital ground plane.
141	TCLK	I	Reference clock(TCLK) input from the 50 MHz crystal oscillator
142	XTAL	O	If using an external oscillator, leave this pin floating. If using an external crystal, connect crystal between TCLK(141) and XTAL(142). See MFB5(pin 107).
143	PLL_RVDDA		Analog power for the Reference DDS PLL. Must be bypassed with a 0.1uF capacitor to pin 144(PLL_RGNDA)
144	PLL_RGNDA		Analog ground for the Reference DDS PLL. Must be directly connected to the analog system ground plane.
145	Reserved		For testing purposes only. Do not connect.
146	SUB_RGNDA		Dedicated pin for the substrate guard ring that protects the Reference DDS. Must be directly connected to the analog system ground plane.
148	VSYNC	I	CRT Vsync input. TTL Schmitt trigger input.
149	SYN_VDD		Digital power for CRT Sync input.
150	HSYNC/CSYNC	I	CRT Hsync or CRT composite sync input. TTL Schmitt trigger input.

Table 4. TFT Panel Interface

PIN #	Name	I/O	Description				
			2pxl/clk 8bit	2pxl/clk 6-bit	1pxl/clk 8-bit	1pxl/clk 6-bit	TFT
6	PD47	O	OB1	-	-	-	
7	PD46	O	OB0	-	-	-	
9	PD45	O	OG1	-	-	-	
10	PD44	O	OG0	-	-	-	
13	PD43	O	OR1	-	-	-	
14	PD42	O	OR0	-	-	-	
15	PD41	O	EB1	-	B1	-	
16	PD40	O	EB0	-	B0	-	
17	PD39	O	EG1	-	G1	-	
19	PD38	O	EG0	-	G0	-	
20	PD37	O	ER1	-	R1	-	
22	PD36	O	ER0	-	R0	-	
23	PD35	O	OB7	OB5	-	-	
24	PD34	O	OB6	OB4	-	-	
25	PD33	O	OB5	OB3	-	-	
26	PD32	O	OB4	OB2	-	-	
27	PD31	O	OB3	OB1	-	-	
28	PD30	O	OB2	OB0	-	-	
29	PD29	O	OG7	OG5	-	-	
31	PD28	O	OG6	OG4	-	-	
32	PD27	O	OG5	OG3	-	-	
34	PD26	O	OG4	OG2	-	-	
35	PD25	O	OG3	OG1	-	-	
36	PD24	O	OG2	OG0	-	-	
37	PD23	O	OR7	OR5	-	-	
38	PD22	O	OR6	OR4	-	-	
39	PD21	O	OR5	OR3	-	-	
42	PD20	O	OR4	OR2	-	-	
46	PD19	O	OR3	OR1	-	-	
47	PD18	O	OR2	OR0	-	-	
48	PD17	O	EB7	EB5	B7	B5	
50	PD16	O	EB6	EB4	B6	B4	
51	PD15	O	EB5	EB3	B5	B3	
52	PD14	O	EB4	EB2	B4	B2	
53	PD13	O	EB3	EB1	B3	B1	
54	PD12	O	EB2	EB0	B2	B0	
55	PD11	O	EG7	EG5	G7	G5	
56	PD10	O	EG6	EG4	G6	G4	
57	PD9	O	EG5	EG3	G5	G3	
62	PD8	O	EG4	EG2	G4	G2	

PIN #	Name	I/O	Description 2pxl/clk 8bit	2pxl/clk 6-bit	1pxl/clk 8-bit	1pxl/clk 6-bit	TFT
63	PD7	O	EG3	EG1	G3	G1	
64	PD6	O	EG2	EG0	G2	G0	
66	PD5	O	ER7	EG5	R7	R5	
67	PD4	O	ER6	ER4	R6	R4	
68	PD3	O	ER5	ER3	R5	R3	
69	PD2	O	ER4	ER2	R4	R2	
70	PD1	O	ER3	ER1	R3	R1	
71	PD0	O	EG2	ER0	R2	R0	
43	PdispE	O	This output provides a panel display enable signal that is active when flat panel data is valid.				
74	PHS	O	This output provides the panel line clock signal.				
73	PVS	O	This output provides the frame start signal.				
44	PCLKA	O	This output is used to drive the flat panel shift clock.				
45	PCLKB	O	Same as PCLKA above. The polarity and the phase of this signal are independently programmable.				
75	Pbias	O	This output is used to turn on/off the panel bias power or controls backlight.				
76	Ppwr	O	This output is used to control the power to a flat panel.				

Table 5. Test Pins

PIN #	Name	I/O	Description
3	PSCAN	I	Enable automatic PCB assembly test. When this input is pulled high, the automatic PCB assembly test mode is entered. An internal pull-down resistor drives this input low for normal operation.
155	SCAN_IN1	I	Scan input 1 used for automatic PCB assembly tesing.
157	SCAN_IN2	I	Scan input 2 used for automatic PCB assembly tesing.
159	SCAN_OUT1	O	Scan output 1 used for automatic PCB assembly tesing.
160	SCAN_OUT2	O	Scan output 2 used for automatic PCB assembly tesing.
153	Reserved		
154	Reserved		

Table 6. VDD / VSS for Core Circuitry, Host Interface, and Panel/Memory Interface

PIN #	Description
65, 40, 33, 12	PVDD4~PVDD1 for panel / memory interface. Connect to +3.3V. Must be the same voltage as the CVDD's
149, 108, 58, 21, 11	SRVDD2-1, CVDD4, CVDD2-1 for core circuitry. Connect to +3.3V. Must be the same voltage as the PVDD's.
158, 151, 140, 126, 114, 72, 61, 49, 41, 30, 18, 8, 1	Digital grounds for core circuiry and panel / memory interface.

1.4 System-level Block Diagram

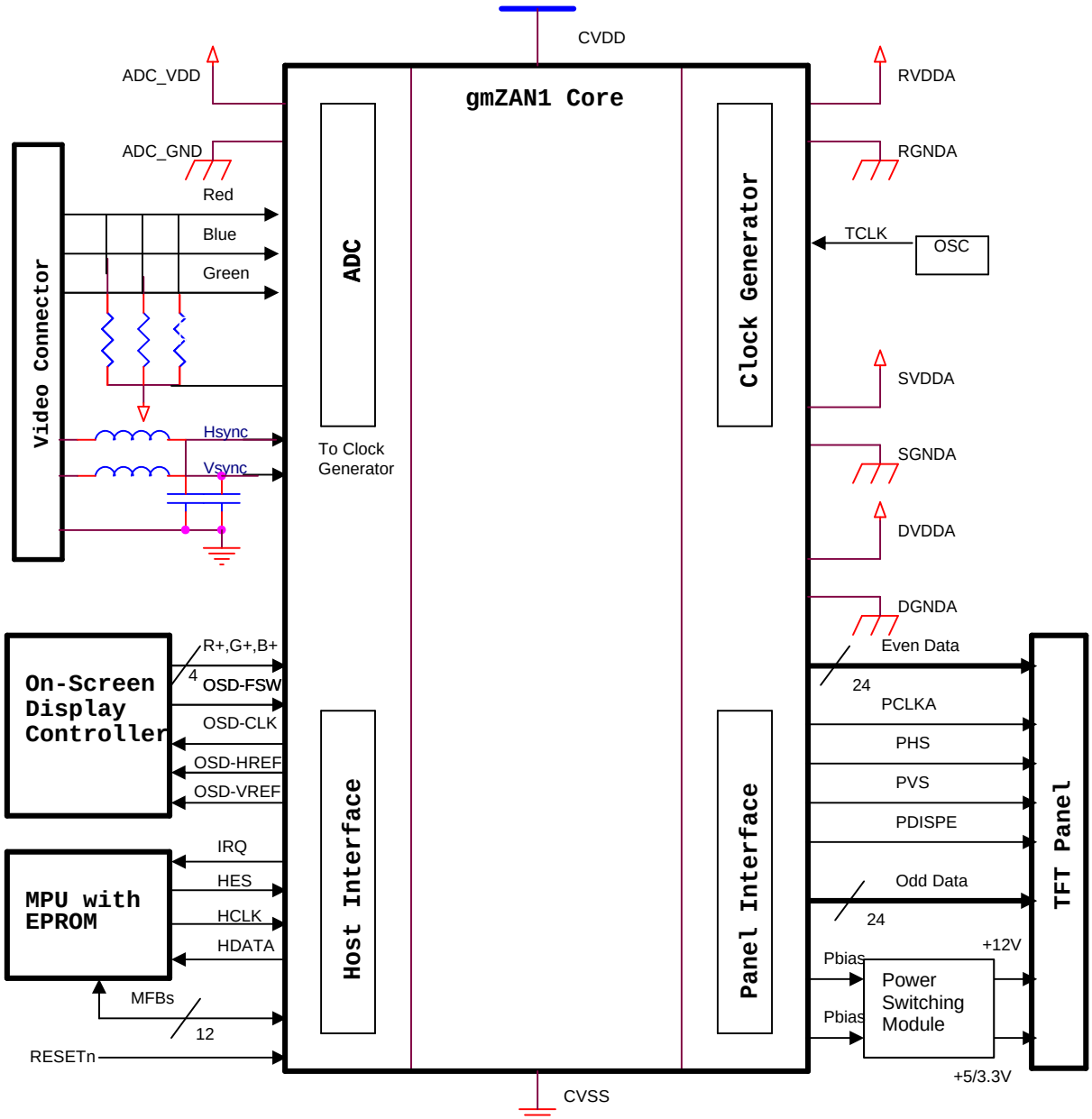


Figure 2. Typical Stand-alone Configuration

1.5 Operating Modes

The Source Clock (also called SCLK in this document) and the Panel Clock are defined as follows:

- The Source Clock is the sample clock regenerated from the input Hsync timing (called clock recovery) by SCLK DDS (direct digital synthesis) and the PLL.
- The Panel Clock is the timing clock for panel data at the single pixel per clock rate. The actual PCLK to the panel may be one-half of this frequency for double-pixel panel data format. When its frequency is different from that of source clock, the panel clock is generated by Destination Clock (or DCLK) DDS/PLL.

There are six display modes: Native, Slow DCLK, Zoom, Downscaling, Destination Stand Alone, and Source Stand Alone.
Each mode is unique in terms of:

- Input video resolution vs. panel resolution
- Source Clock frequency / Panel Clock frequency ratio
- Source Hsync frequency / Panel Hsync frequenc ratio
- Data source (analog RGB, panel background color, on-chip pattern generator

1.5.1 Native

Panel Clock frequency = Source Clock frequency
Panel Hsync frequency = Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is the same as the panel resolution and the input data clock frequency is within the panel clock frequency specification of the panel being used.

1.5.2 Slow DCLK

Panel Clock frequency < Source Clock frequency
Panel Hsync frequency = Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is the same as the panel resolution, but the input data clock frequency is exceeds the panel clock frequency specification of the panel being used. The panel clock is scaled to the Source Clock, and the internal data buffers are used to spread out the timing of the input data by making use of the large CRT blanking time to extends the panel horizontal display time.

1.5.3 Zoom

Panel Clock frequency > Source Clock frequency
Panel Hsync frequency > Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is less than the panel resolution. The input data clock is then locked to the pnael clock, which is at a higher frequency. The input data is zoomed to the panel resolution.

1.5.4 Downscaling

Panel Clock frequency < Source Clock frequency
Panel Hsync frequency < Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is greater than the panel resolution, to provide enough of a display to enable the user to recover to a supported resolution. The input clock is operated at a frequency less than that of the input pixel rate(under-sampled horizontally) and the scaling filter is used to drop input lines. In this mode, zoom scaling must be disabled

1.5.5 Destination Stand Alone

Panel Clock = DCLK in open loop (not locked)
Panel Hsync frequency = DCLK frequency / (Destination Htotal register value)
Panel Vsync frequency = DCLK frequency / (Dest. Htotal register value * Dest. Vtotal register value)

This mode is used when the input is changing or not available. The OSD may still be used as in all other display modes and stable panel timing signals are produced. This mode may be automatically set when the gmZAN1 detects input timing changes that could cause out- of-spec operation of the panel.

1.5.6 Source Stand Alone

Panel Clock = DCLK in open loop (not locked to input Hsync)
Panel Hsync frequency = SCLK frequency / (Source Htotal register value)
Panel Vsync frequency = SCLK frequency / (Source Htotal register value *Source Vtotal register value)

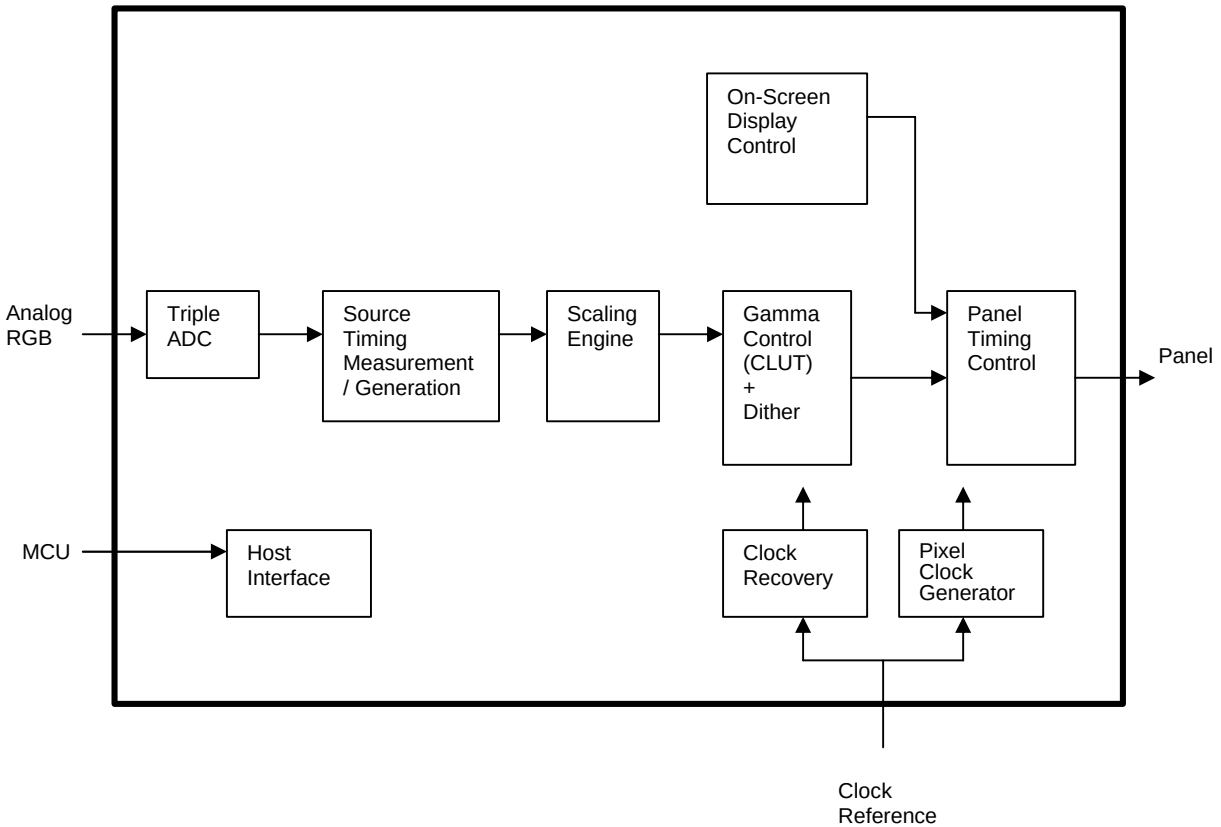
This mode is used to display the pattern generator data. This mode may be useful for testing an LCD panel on the manufacturing line (color temperature calibration, etc.).

2. FUNCTIONAL DESCRIPTION

Figure 3 below shows the main functional blocks inside the gmZAN1

2.1 Overall Architecture

Figure 3. Block Diagram for gmZAN1



2.2 Clock Recovery Circuit

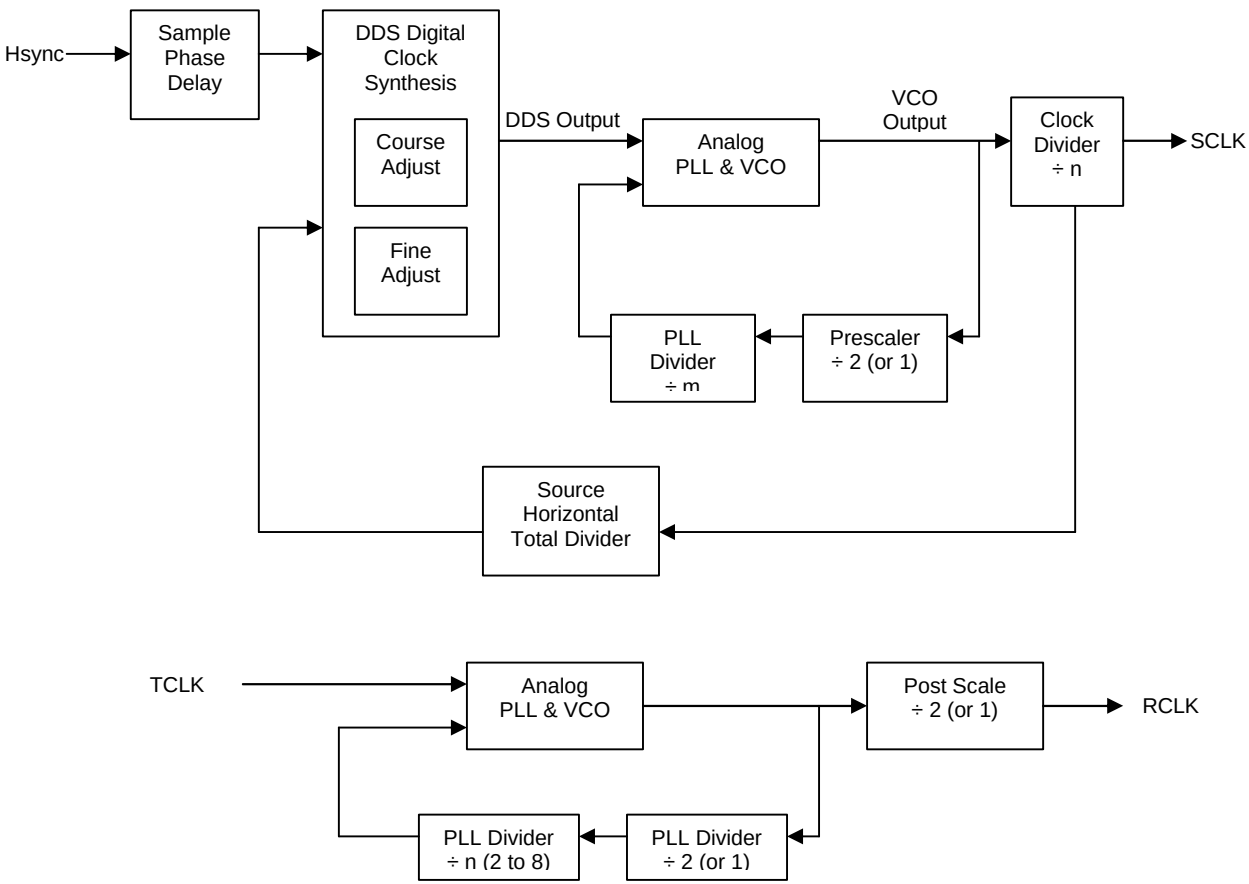
The gmZAN1 has a built-in clock recovery circuit. This circuit consists of a digital clock synthesizer and an analog PLL. The clock recovery circuit generates the clock used to sample analog RGB data (SCLK or source clock). This circuit is locked to the HSUNC of the incoming video signal. The RCLK generated from the TCLK input is used as a reference clock.

The clock recovery circuit adjusts the SCLK period so that the feedback pulse generated every SCLK period multiplied by the Source Horizontal Total value (as programmed into the registers) locks to the rising edge of the Hsync input. Even though the initial SCLK frequency and the final SCLK frequency are as far apart as 60MHz , locking can be achieved in less than 1ms across the operation voltage/temperature range.

The SCLK frequency (1/SCLK period) can be set to the range of 10-to-135 MHz. Using the DDS (direct digital synthesis) technology the clock recovery circuit can generate any SCLK clock frequency within this range.

The pixel clock (DCLK or destination clock) is used to drive a panel when the panel clock is different from SCLK (or SCLK/2). It is generated by a circuit virtually identical to the clock recovery circuit. The difference is that DCLK is locked to SCLK while SCLK is locked to the Hsync input. DCLK frequency divided by N is locked to SCLK frequency divided by M. The value M and N are calculated and programmed in the register by firmware. The value M should be close to the Source Htotal value.

Figure 4. Clock Recovery Circuit



The table below summarizes the characteristics of the clock recovery circuit.

Table 7. Clock Recovery Characteristics

	Minimum	Typical	Maximum
SCLK Frequency	10MHz		135 MHz
Sampling Phase Adjustment		0.5 ns/step, 64 steps	

Patented digital clock synthesis technology makes the gmZAN1 clock circuits very immune to temperature/voltage drift.

2.2.1 Sampling Phase Adjustment

The ADC sampling phase is adjusted by delaying the Hsync input at the programmable delay cell inside the gmZAN1. The delay value can be adjusted in 64 steps, 0.5 ns/step. The accuracy of the sampling phase is checked by the gmZAN1 and the "score" can be read in a register. This feature will enable accurate auto-adjustment of the ADC sampling phase.

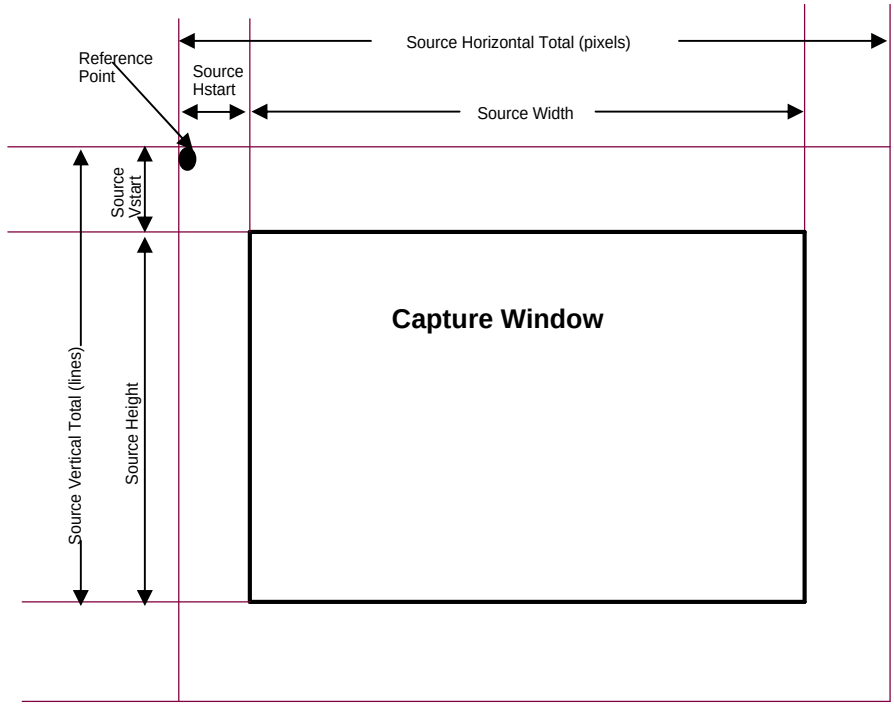
2.2.2 Source Timing Generator

The STG module defines a capture window and sends the input data to the data path block. The figure below shows how the window is defined.
For the horizontal direction, it is defined in SCLKs (equivalent to a pixel count). For the vertical direction, it is defined in lines.
All the parameters in the figure that begin with "Source" are programmed into the gmZAN1 registers.
Note that the vertical total is solely determined by the input.
The reference point is as follows:

- The first pixel of a line: the pixel whose SCLK rising edge sees the transition of the HSYNC polarity from low to high.
- The first line of a frame: the line whose HSYNC rising edge sees the transition of the VSYNC polarity from low to high.

The gmZAN1 also supports the use of analog composite sync and digital sync signals as described in Section 2.3.2

Figure 5. Capture Window



2.3 Analog-to-Digital Converter

2.3.1 Pin Connection

The RGB signals are to be connected to the gmZAN1 chip as described in Table 8 and Table 9.

Table 8. Pin Connection for RGB Input with Hsync/Vsync

GmZAN1 Pin Name (Pin Number)	CRT Signal Name
Red+(#95)	Red
Red- (#94)	N/A (Tie to Analog GND for Red on the board)
Green+(#91)	Green
Green- (#90)	N/A (Tie to Analog GND for Green on the board)
Blue+(#87)	Blue
Blue- (#86)	N/A (Tie to Analog GND for Blue on the board)
HSYNC/CS (#150)	Horizontal Sync
VSYNC (#148)	Vertical Sync

Table 9. Pin Connection for RGB Input with Composite Sync

GmZAN1 Pin Name (Pin Number)	CRT Signal Name
Red+(#95)	Red
Red- (#94)	N/A (Tie to Analog GND for Red on the board)
Green+(#91)	Green When using Sync-On-Green this signal also carries the sync pulse.
Green- (#90)	N/A (Tie to Analog GND for Green on the board)
Blue+(#87)	Blue
Blue- (#86)	N/A (Tie to Analog GND for Blue on the board)
HSYNC/CS (#150)	Digital composite sync. Not applicable for Sync-On-Green

The gmZAN1 chip has three ADC's (analog-to-digital converters), one for each color (red, green, and blue). Table 10 summarizes the characteristics of the ADC.

Table 10. ADC Characteristics

	MIN	TYP	MAX	NOTE
RGB Track & Hold Amplifiers				
Band Width		160MHz		
Settling Time to 1/2%		8.5ns		Full Scale Input = 0.75V, BW=160MHz(*)
Full Scale Adjust Range @ R,G,B Inputs	0.45V		0.95V	
Full Scale Adjust Sensitivity		+/-1 LSB		Measured @ ADC Output (**)
Zero Scale Adjust Range				For a larger DC offset from an external video source, the AC coupling feature is used to remove the offset.
Zero Scale Adjust Sensitivity		+/-1 LSB		Measured @ ADC Output
ADC+RGB Track & Hold Amplifiers				
Sampling Frequency (fs)	20MHz		110MHz	
DNL			+/- 0.9LSB	fs = 80 MHz
INL		+/- 1.5LSB		fs = 80 MHz
Channel to Channel Matching		+/- 0.5LSB		
Effective Number of Bits (ENOB)		7 Bits		fin = 1MHz, fs=80 MHz Vin= -1db below full scale=0.75V
Power Dissipation		400mW		fs=110 MHz, Vdd=3.3V
Shut Down Current			100uA	

(*) Guaranteed by design (**) Independent of full scale R,G,B input

The gmZAN1 ADC has a built-in clamp circuit. By inserting series capacitors (about 10 nF) the DC offset of an external video source can be removed. The clamp pulse position and width are programmable.

2.3.2 Sync. Signal Support

The gmZAN1 chip supports digital separate sync (Hsync/Vsync), digital composite sync, and analog composite sync (also known as sync-on-green). All sync types are supported without external sync separation / extraction circuits.

Digital Composite Sync
The types of digital composite sync inputs supported are:
- ✍ OR/AND type: No Csync pulses toggling during the vertical sync period
- ✍ XOR type: Csync polarity changes during the vertical sync period

The gmZan1 provides enough sync status information for the firmware to detect the digital composite sync type.

Sync-On-Green (Analog Composite Sync)
The voltage level of the sync tip during the vertical sync period can be either –0.3V or 0V

2.3.3 Display Mode Support

A mode calculation utility (MODECALC.EXE) provided by Genesis Microchip may be run before compilation of the firmware to determine which input modes can be supported. Refer to firmware documents for more details.

2.4 Input Timing Measurement

As described in section 2.2.2 above, input data is sent from the analog-to-digital converter to the source timing generator (STG) block. The STG block defines a capture window (Figure5).

The input timing measurement block consists of the source timing measurement (STM) block and interrupt request (IRQ) controller. Input timing parameters are measured by the STM block and stored in registers. Some input conditions will generate an IRQ to an external micro-controller. The IRQ generating conditions are programmable.

2.4.1 Source Timing Measurement

When it receives the active CRT signal (R,G,B and Sync signals) the Source Timing Measurement unit begins measuring the horizontal and vertical timing of the incoming signal using the sync signals and TCLKi as a reference. Horizontal measurement occurs by measuring a minimum and a maximum value for each parameter to account for TCLKi sampling granularity. The measured value is updated every line. Vertical parameters are measured in terms of horizontal lines. The trailing edge of the Hsync input is used to check the polarity of the Vsync input.
The table below lists all the parameters that may be read in the source timing measurement (STM) registers of the gmZAN1.

Table 11. Input Timing Parameters Measured by the STM Block

Parameter	Unit	Updated at:
HSYNC Missing	N/A	Every 4096 TCLKs and every 80ms (2-bits)
VSYNC Missing	N/A	Every 80ms
HSYNC/VSYNC Timing Change	N/A	When the horizontal period delta or the vertical period delta to the previous line / frame exceeds the threshold value (programmable).
HSYNC Polarity	Positive/Negative	After register read
VSYNC Polarity	Positive/Negative	Every frame
Horizontal Period Min/Max	TCLKs and SCLKs	After register read
HSYNC High Period Min/Max	TCLKs	After register read
Vertical Period	Lines	Every frame
VSYNC High Period	Lines	Every frame
Horizontal Display Start	SCLKs	Every frame
Horizontal Display End	SCLKs	Every frame
Vertical Display Start	Lines	Every frame
Vertical Display End	Lines	Every frame
Interlaced Input Detect	N/A	Every frame
CRC Data/Line Data	N/A	Every frame
CSYNC Detect	N/A	Every 80ms

The display start/end registers store the first and the last pixels/lines of the last frame that have RGB data above a programmed threshold.
The reference point of the STM block is the same as that of the source timing generator (STG) block:

- The first pixel: the pixel whose SCLK rising edge sees the transition of the HSYNC polarity from low to high.
- The first line: the line whose HSYNC rising edge sees the transition of the VSYNC polarity from low to high.

The CRC data and the line data are used to detect a test pattern image sent to the gmZAN1 input port.

2.4.2 IRQ Controller

Some input timing conditions can cause the gmZAN1 chip to generate an IRQ. The IRQ-generating conditions are programmable, as given in the following table.

Table 12. IRQ-Generation Conditions

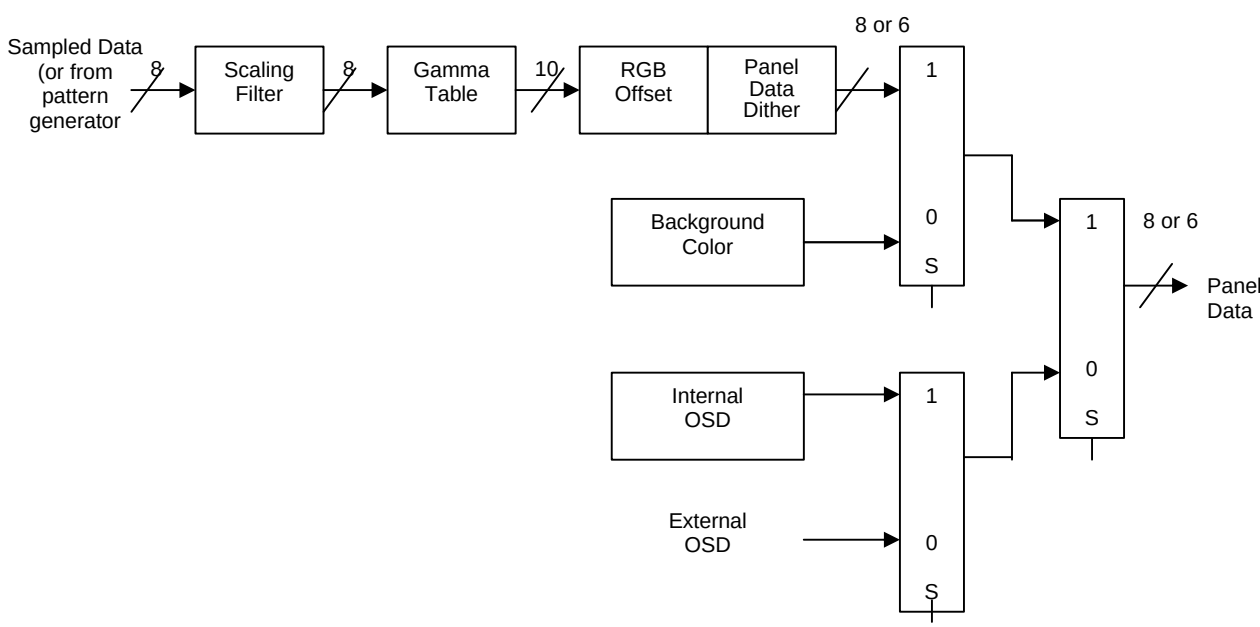
IRQ Event	Remark
Timing Event	One of the three events: ✍ Leading edge of Vsync input, ✍ Panel line count (the line count is programmable), ✍ Every 10ms Only one event may be selected at a time.
Timing Change	Any of the following timing changes: ✍ Sync loss, ✍ DDS tracking error beyond threshold, ✍ Horizontal/vertical timing change beyond threshold Threshold values are programmable.

Reading the IRQ status flags will not affect the STM registers.
Note that if a new IRQ event occurs while the IRQ status register is being read, the IRQ signal will become inactive for minimum of one TCLK period and then get re-activated. The polarity of the IRQ signal is programmable.

2.5 Data Path

The data path block of gmZAN1 is shown in Figure 6.

Figure 6. gmZAN1 Data Path



2.5.1 Scaling Filter

The gmZAN1 scaling filter uses an advanced adaptive scaling technique proprietary to Genesis Microchip Inc. and provides high quality scaling of real time video and graphics images. This is Genesis' third generation scaling technology that benefits from the expertise and feedback gained by supporting a wide range of solutions and applications.

2.5.2 Gamma Table

The gamma table is used to adjust the RGB data for the individual display characteristics of the TFT panel. The overall gamma of the display may be set, as well as separate corrections for each of the three display channels. In addition, the gamma table may be used for contrast, brightness, and white balance (temperature) adjustments. The lookup table has an 8-bit input (256 different RGB entries) and produces a 10-bit output.

2.5.3 RGB Offset

The RGB offsets provide a simple shift (positive or negative) for each of the three color channels. This may be used as a simple brightness adjustment within a limited range. The data is clamped to zero for negative offsets, and clamped to FFh for positive offsets. This adjustment is much faster than recalculating the gamma table, and could be used with the OSD user controller to provide a quick brightness adjust. An offset range of plus 127*4 to minus 127*4 is available.

2.5.4 Panel Data Dither

For TFT panels that have fewer than eight bits for each R,G,B input, the gmZAN1 provides ordered and random dithering patterns to help smoothly shade colors on 6-bit panels.

2.5.5 Panel Background Color

A solid background color may be selected for a border around the active display area. The background color is most often set to black.

2.6 Panel Interface

The gmZAN1 chip interfaces directly with all of today's commonly used active matrix flat panels with 640x480, 800x600 and 1024x768 resolutions. The resolution and the aspect ratio are NOT limited to specific values.

2.6.1 TFT Panel Interface Timing Specification

The TFT panel interface timing parameters are listed in Table 13 below. Refer to three timing diagrams of Figure 7 and Figure 8 for the timing parameter definition. All aspects of the gmZAN1 interface are programmable. For horizontal parameters, Horizontal Display Enable Start, Horizontal Display Enable End, Horizontal Sync Start and Horizontal Sync End are programmable. Vertical Display Enable Start, Vertical Display Enable End, Vertical Sync Start and Vertical Sync End are also fully programmable.
In order to maximize panel data setup and hold time, the panel clock (PCLKA, PCLKB) output skew is programmable. In addition, the current drive strength of the panel interface pins is programmable.

Table 13. gmZAN1 TFT Panel Interface Timing

Signal Name			Min	Typical	Max	Unit
PVS	Period	t1	0	16.67	2048 -	lines ms
	Frequency			60	-	Hz
	Front porch	t2	0		2048	lines
	Back porch	t3	0		2048	lines
	Pulse width	t4	0		2048	lines
	PdispE	t5	0	Panel height	2048	lines
	Disp. Start from VS	t6	0		2048	lines
	PVS set up tp PHS	t18	1		2048	PCLK *1
	PVS hold from PHS	t19	1		2048	PCLK *1
PHS	Period	t7	0		2048 [1024	PCLK *1
	Front porch	t8	0		2048	PCLK *1
	Back porch	t9	0		2048	PCLK *1
	Pulse width	t10	0		2048	PCLK *1
	PdispE	t11	0	Panel width	2048 [1024]	PCLK *1
	Disp. Start fom HS	t12	0		2048	PCLK *1
PCLKA, PCLKB*4	Frequency	t13			120 [60]	MHz
	Clock (H) *2	t14	DCLK/2-3 [DCLK-3]		DCLK/2-2 [DCLK-2]	ns
	Clock (L) *2	t15	DCLK/2-3 [DCLK-3]		DCLK/2-2 [DCLK-2]	ns
	Type		-	One pxl/clock [two pxl/clock]	-	
Data	Set up *3	t16	DCLK/2-5 [DCLK-5]		DCLK/2-2 [DCLK-2]	ns
	Hold *3	t17	DCLK/2-5 [DCLK-5]		DCLK/2-2 [DCLK-2]	ns
	width		3 bits	18 bits [36 bits]	24 bits [48 bits]	bits/pixel

NOTE: Numbers in [ ] are for two pixels/clock mode.

NOTE: The drive current of the panel interface signals is programmable as shown in Table 1. The drive current is to be programmed through the API upon chip initialization. Output current is programmable from 2 mA to 20mA in increments of 2 mA. Drive strength should be programmed to match the load presented by the cable and input of the panel. Values shown are based on a loading of 20pF and a drive strength of 8 mA.

NOTE *1: The PCLK is the panel shift clock.

NOTE *2: The DCLK stands for Destination Clock (DCLK) period. Is equal to:

-PCLK period in one pixel/clock mode,

-twice the PCLK period in two pixels/clock mode.

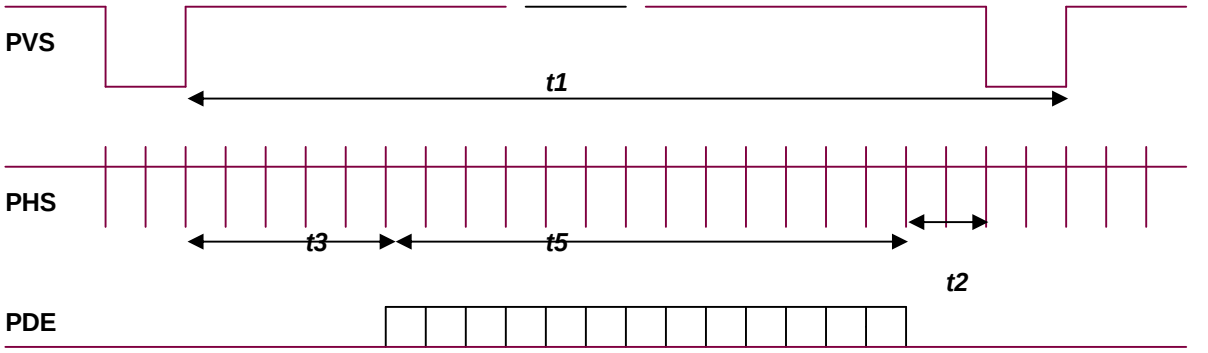
NOTE *3: The setup/hold time spec. for PCLK also applies to PHS and PdispE. The setup time (t16) and the hold time (t17) listed in this table are for the case in which no clock-to-data skew is added. The PVS/PHS/PdispE/Pdata signals are asserted on the rising edge of the PCLK. The polarity of the PCLK and its skew are programmable. Clock to Data skew can be adjusted in sixteen 800-ps increments. In combination with the PCLK polarity inversion, the clock-to-data phase can be adjusted in total of 31 steps.

NOTE *4: The polarity of the PCLKA and the PCLKB are independently programmable.

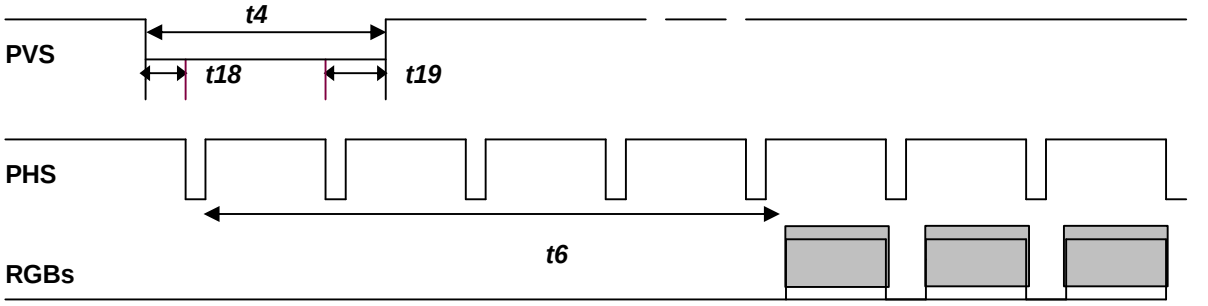
The microcontroller must have all the timing parameters of the panel used for the monitor. The parameters are to be stored in a non-volatile memory. As can be seen from this table, the wide range of timing programmability of the gmZAN1 panel interface makes it possible to support various kinds of panels known today:

Figure 7. timing Diagrams of the TFT Panel Interface (One pixel per clock)

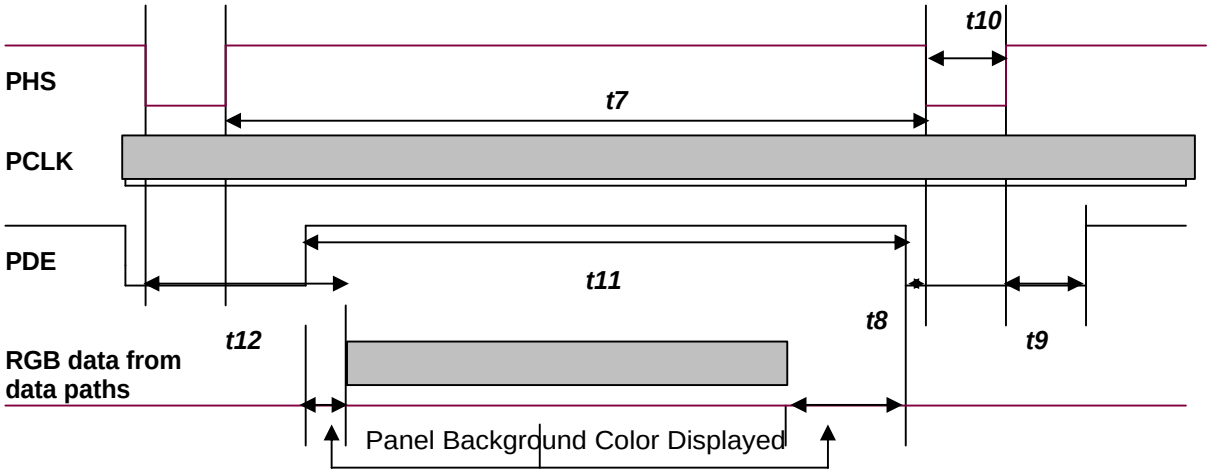
(a) Vertical size in TFT



(b) Vsync width and display position in TFT



(c) Horizontal size in TFT



(d) Hsync width in TFT

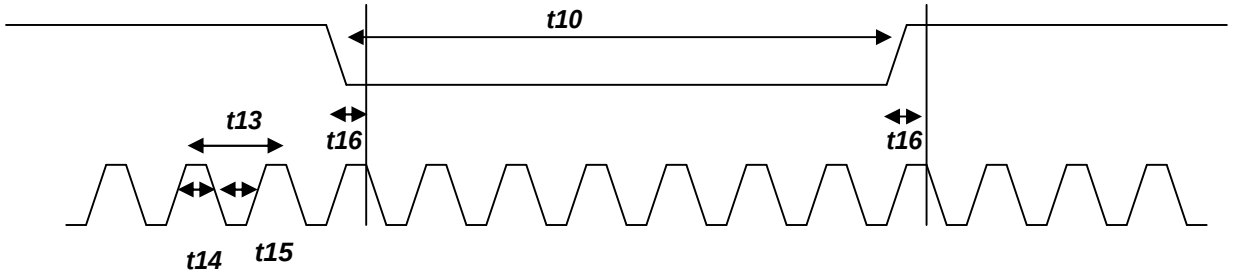
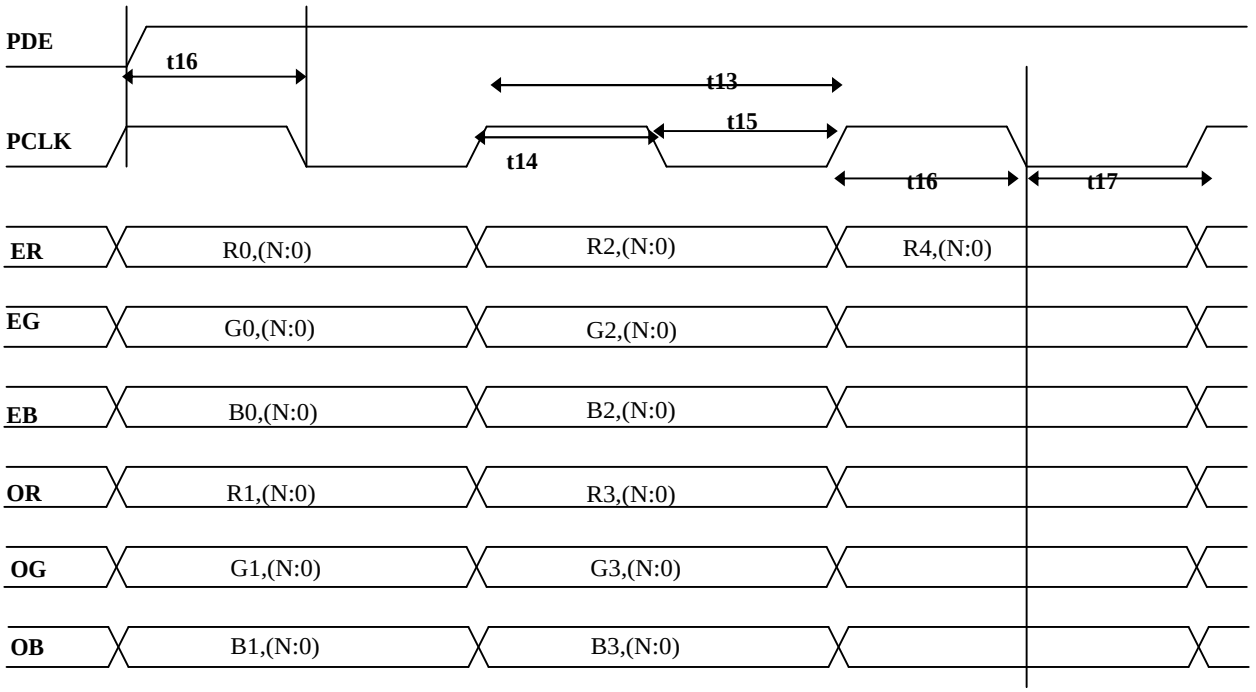
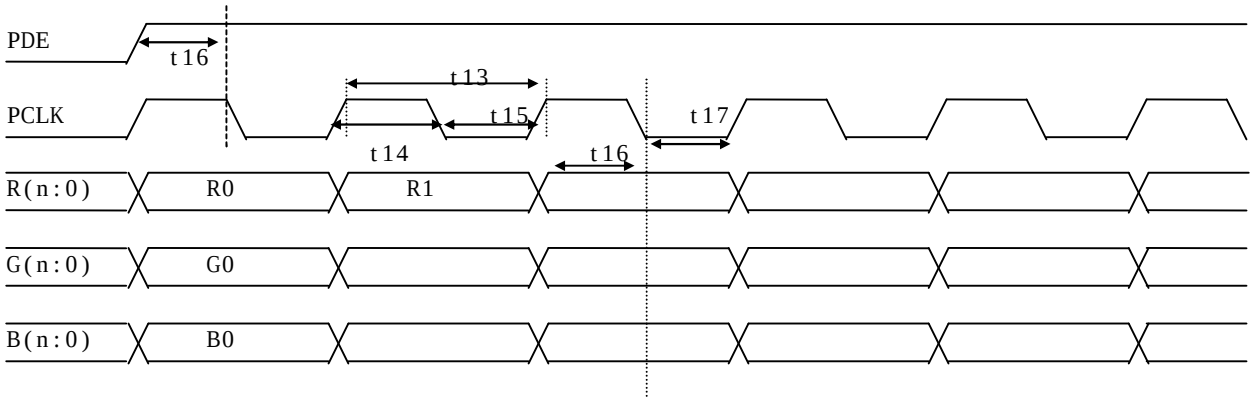


Figure 8. Data latch timing of the TFT Panel Interface

(a) Two pixel per clock mode in TFT



(b) One pixel per clock mode in TFT



2.6.2 Power Manager

LCD panels require logic power, panel bias power, and control signals to be sequenced in a specific order, otherwise severe damage may occur and disable the panel permanently. The gmZAN1 has a built in power sequencer (Power Manager) that prevents this kind of damage.

The Power Manager controls the power up/down sequences for LCD panels within the four states described below. See the timing diagram Figure 9.

2.6.2.1 State 0 (Power Off)

The Pbias signal and Ppower signal are low (inactive). The panel controls and data are forced low. This is the final state in the power down sequence. PM is kept in state 0 until the panel is enabled.

2.6.2.2 State 1 (Power On)

Intermediate step 1. The Ppower is high (active), the Pbias is low (inactive), and the panel interface is forced low (inactive).

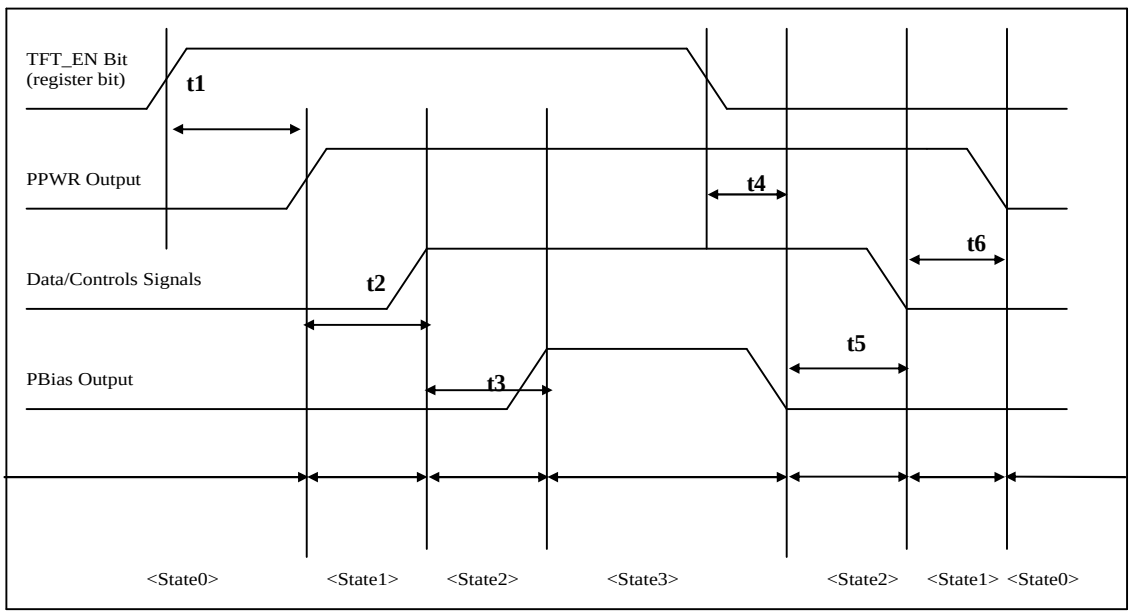
2.6.2.3 State 2 (Panel Drive Enabled)

Intermediate step 2. The Ppower is high (active), the Pbias is low (inactive), and the panel interface is active.

2.6.2.4 State 3 (Panel Fully Active)

This is the final step in the power up sequence, with Ppower and Pbias high (active), and the panel interface active. PM is kept in this state until the internal TFT_Enable signal controlled by Panel Control register is disabled. The panel can be disabled through either an API call under program control or automatically by the gmZAN1 to prevent damage to the panel.

Figure 9. Panel Power Sequence



In Figure 9 above, t2=t6 and t3=t5. t1,t2,t3 and t4 are independently programmable from one to eight steps in length. The length of each step is in the range of 511 * X* (TCLKi cycle) or (TCLKi cycle) * 32193 *X, where X is any positive integer value equal to or less than 256. TCLKi is the reference clock to the gmZAN1 chip, and ranges from 14.318 MHz to 50 MHz in frequency. This programmability provides enough flexibility to meet a wide range of power sequencing requirements by various panels.

2.6.3 Panel Interface Drive Strength

As mentioned previously, the gmZAN1 has programmable output pads for the TFT panel interface. Three groups of panel interface pads (panel clock, data, and control) are independently controllable and are programmed using API calls. See the API reference manual for details.

Table 14. Panel Interface Pad Drive Strength

Value (4 bits)	Drive Strength in mA
0	Outputs are in tri-state condition
1	2mA
2	4mA
3	6mA
4	8mA
5	10mA
6	12mA
7	14mA
8	16mA
9	18mA
10,11,12,13,14,15	20mA

2.7 Host Interface

The host microcontroller interface of the gmZAN1 has two modes of operation: gmB120 compatible mode, and a 4-bit serial interface mode.

- GmB120 compatible mode-Four signals consisting of 1 data bit, a frame synchronization signal, a clock signal and an Interrupt Request signal (IRQ). This mode is entered when a pull-down resistor is not connected to MFB6(pin number 106).
- 4-bit serial interface mode-Same as gmB120 compatible mode with the addition of three data bits so that four data bits are transferred on each clock edge. This mode is entered when a (10K ohm) pull-down resistor is connected to MFB6(pin number 106).

When the chip is configured for 4-bit host interface, MFB9:7 are used as HDATA3:1 and HDATA is used as HDATA0. For instruction, Read Data, or Write Data, the data order is D3:0, D7:4, D11:8, The burst mode operation then uses three clocks (instead of twelve) for each 12-bit data (or address) transmission.

In both modes, a reset pin sets the chip to a known state when the pin is pulled low. The RESETn pin must be low for at least 100ns after the CVDD has become stable (between +3.15V and +3.45V) in order to reset the chip to a known state.

The gmZAN1 chip has an on-chip pull-down resistor in the HFS input pad. No external pull-up is required. The signal stays low until driven high by the microcontroller.

2.7.1 Serial Communication Protocol

In the serial communication between the microcontroller and the gmZAN1, the microcontroller always acts as an initiator while the gmZAN1 is always the target. The following timing diagram describes the protocol of the serial channel of the gmZAN1 chip.

Figure 10. Timing Diagram of the gmZAN1 Serial Communication

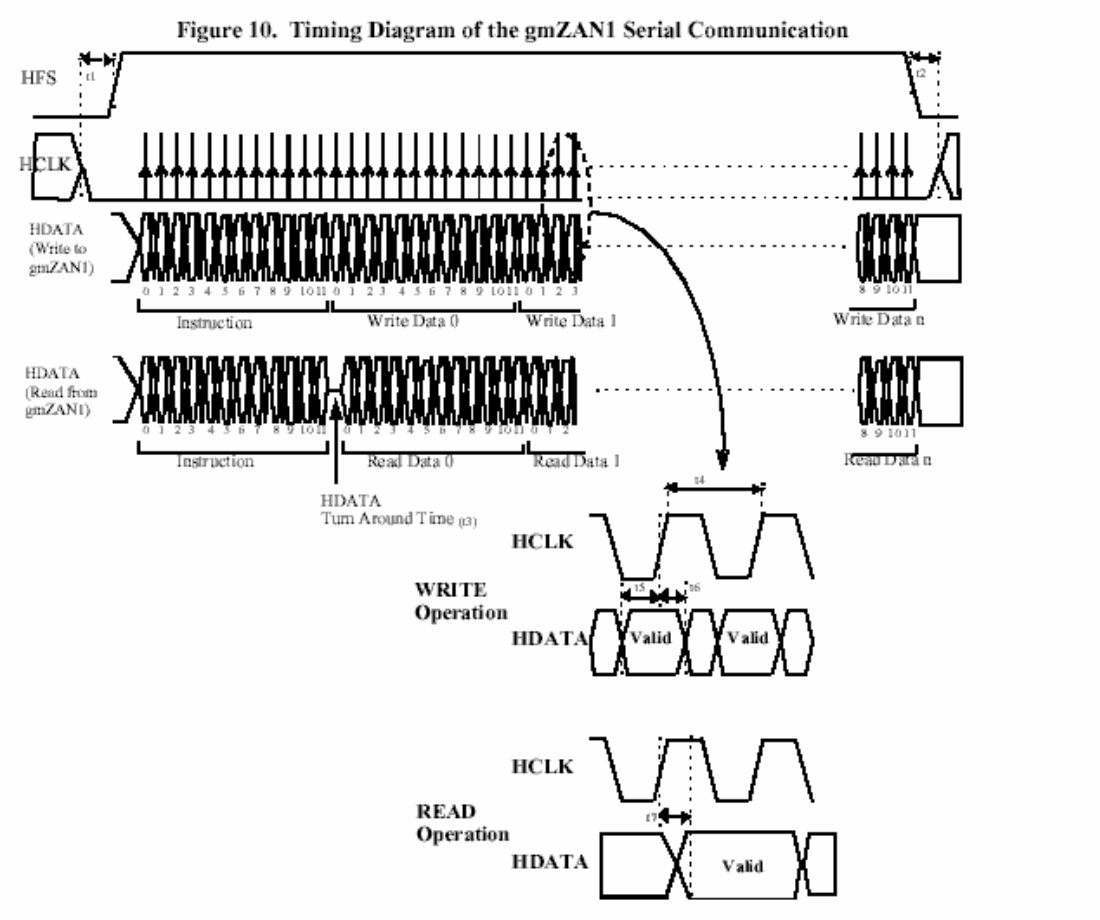


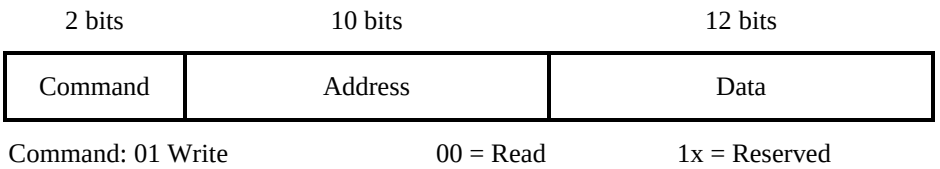
Table 15 summarizes the serial channel specification of the gmZAN1. Refer to Figure 10 for the timing parameter definition.

Table 15. gmZAN1 Serial Channel Specification

Parameter	Min.	Typ.	Max.
Word Size (Instruction and Data)	---	12 bits	---
HCLK low to HFS high (t1)	100 ns		
HFS low to HCLK inactive (t2)	100 ns		
HDATA Write to Read Turnaround Time (t3)	1 HCLK cycle		1 HCLK cycle
HCLK cycle (t4)	100 ns		
Data in setup time (t5)	25 ns		
Data in hold time (t6)	25 ns		
Data out valid (t7)	5 ns		10

In the read operation, the microcontroller (Initiator) issues an instruction lasting 12 HCLKs. After the last bit of the command is transferred to the gmZAN1 on the 12^{th} clock, the microcontroller must stop driving data before the next rising edge of HCLK at which point the gmZAN1 will start driving data. At the 13^{th} rising edge of HCLK, the gmZAN1 will begin driving data.

Figure 11. Serial Host Interface Data Transfer Format



Note that when the chip is configured for a 4-bit host interface, MFB9:7 are used as HDATA 3:1 and HDATA is used as HDATA0. The command and address information are transferred as Address 1:0+Command1:0, Address5:2 and Address9:6. The data information is transferred as Data3:0,Data 7:4, Data 11:8. Thus, in this mode the HDATA pin carries Command0, Address2, Address6, Data0, Data4 and Data8.
On the gmZAN1 reference design board, the microcontroller toggles the HCLK and HDATA lines under program control. Genesis Microchip provides API calls to facilitate communication between the microcontroller and the gmZAN1. Refer to the API reference manual for details.

2.7.2 Multi-Function Bus (MFB)

The Multi-Function Bus provides additional 12 pins that are used as general purpose input and output (GPIO) pins. Each pin can be independently configured as input or output.
MFB pins 9 through 5 have special functions:

- When a 10K ohm pull-down resistor is connected to MFB6 (MFB6 has an internal pull-up resistor) MFB9:7 are used as host data bits HDATA3:1.
- When a 10K ohm pull-down resistor is connected to MFB5 (MFB5 has an internal pull-up resistor) a crystal can be placed between XTAL and TCLK instead of using an external oscillator for the TCLK input.

Note that all pins on the multi-function bus MFB11:0 are internally pulled-up.

2.8 On-Screen Display Control

The gmZAN1 chip has a built-in OSD (On-Screen Display) controller with an integrated font ROM. The chip also supports an external OSD controller for monitor vendors to maintain a familiar user interface.
The internal and external OSD windows may be displayed anywhere the panel Display Enable is active, regardless of whether the panel would otherwise display panel background color or active data.

2.8.1 OSD Color Map

Both the internal and external OSD display use a 16 location SRAM block for the color programming. Each color location is a twelve-bit value that defines the upper four bits of each of the 8 bit Red, Blue and Green color components as follows:

- D3:0 Blue; D7:4 of blue component of color
- D7:4 Green; D7:4 of green component of color
- D11:8 Red; D7:4 of red component of color

To extend the 4-bit color value programmed to the full 8 bits the following rule is applied: if any of the upper four color bits are a “1”, then R (G, B) data 3:0=1111b, otherwise R (G, B) data 3:0=0000b

2.8.2 On-Chip OSD Controller

The internal OSD uses a block of SRAM of 1536x12 bits and a ROM of 1024x12 bits. The SRAM is used for both the font data and the character-codes while the ROM is used to store the bit data for 56 commonly used characters. The font data is for 12 pixel x 18 line characters, one bit per pixel. The font data starts at address zero. The character-codes start at any offset (with an address resolution of 16) that is greater than the last location at which font data has been written . It is the programmer’s responsibility to ensure that there is no overlap between fonts and character-codes. This implementation results in a trade-off between the number of unique fonts on-screen at any one time and the total number of characters displayed. For example, one configuration would be 98 font maps (56 fonts in ROM and 42 fonts in SRAM) and 768 characters (e.g. in a 24x32 array).

The on-chip OSD of the gmZAN1 can support a portrait mode (in which the LCD monitor screen is rotated 90 degrees). In this portrait mode, all the fonts must be loaded in the SRAM, because the ROM stores fonts for a landscape mode (typical orientation) only. The font size in the portrait mode is 12 pixels by 12 lines. As is the case in landscape mode, the SRAM is divided into a font storage area and a character code storage area. For example, 64 fonts can be stored in RAM and an OSD window of 768 characters (such as 24x32) can still be displayed.

The first address of SRAM to be read for the first character displayed (upper left corner of window)is also programmable, with an address resolution of 16 (8-bits as the top bits of the 12-bit SRAM address). The character-code is a 12-bit value used as follows:

- D6:0 font-map select, this is the top seven bits of the address for the first line of font bits
- D8:7 Background color, 00=bcolor0, 01=bcolor1, 10=bcolor2, 11=transparent background
- D10:9 Foreground color (0, 1, 2 or 3)
- D11 Blink enable if set to 1, otherwise no blink

Although the OSD color map has room for sixteen colors, only seven are used by the internal OSD: three background colors and four foreground colors.

The blink rate is based on either a 32 or 64 frame cycle and the duty cycle may be selected as 25/75/50/50% or 75/25%. The 2-bit foreground and background attributes directly select the color (there is no indirect “look-up”, i.e. there is no TMASK function). The 2560 addresses of the ROM/SRAM are mapped as 10 segments of 256 contiguous addresses each, to the OSD memory page of 100h-1FFh in the host interface. A 4-bit register value selects the segment to map to the host R/W page.

The character cell height and width are programmable from 5-66 pixels or 2-65 lines. The X/Y offset of the font bit-map upper-left pixel relative to the upper-left pixel of the character cell is also programmable from 0-63 (pixels or lines). The OSD window height and width in characters/rows is programmable from 1-64.

The Start X/Y position for the upper left corner of the OSD window is programmable (in panel pixels and lines) from 0-2047. There is an optional window border (equal width on all four sides of the window) or a window shadow (the window bottom and right side) the border is a solid color that is selected by an SRAM location as RGB444. The border width may be set as 1, 2, 4 or 8 pixels/lines. These parameters are summarized in Figure 12 and Table 16.
The Font Data D11:0 for each line is displayed with bit D11 first (leftmost) and D0 last.
The reference point for the OSD start is always the upper left corner of the Panel display, which is the start (leading edge) of Panel Display Enable for both Horizontal and Vertical timing.

The OSD Window start position sets the location of the first pixel of the OSD to display, including any border. That is; if the border is enabled, the start of the character display of the OSD is offset from the OSD start position by the width/height of the border.

To improve the appearance and make it easy to find the OSD window on the screen, the user may select optional shadowing (3D effect). The “Shadow” feature operates in the same manner as in the B120; that is, it produces a region of half intensity (scaler data) pixels of the same width and height as the OSD window, but offset to the right and down by 8 pixels/lines (the border width setting has no effect). OSD foreground and background colors always cover the OSD window region of the “shadow”, but transparent background pixels in the OSD will show the half intensity panel data. Therefore, it is not recommended to use both the “shadow” feature and transparent background OSD pixels together. The ”shadow” does not change the intensity of any panel background color over which it may be located. The border and shadow are mutually exclusive, only one may be selected at a time.

The OSD window is not affected by the scaling operation. The size will stay the same whether the source input data is scaled or not.

2.9 TCLK Input

The source timing is measured by using the TCLK input as a reference. Also, the reference clock to the on-chip PLLs are derived from the TCLK. It is therefore crucial to have a jitter-free clock reference.
Table 19 shows the requirements for the TCLK signal.

Table 19. TCLK Specification

Frequency	20 MHz to 50 MHz
Jitter	250 ps maximum
Rise Time (10% to 90%)	5 ns
Duty Cycle	40-60

There is also an option to use a crystal (instead of an oscillator) for the TCLK input. This option is selected by pulling down MFB5 and connecting the crystal between XTAL and TCLK.

3. ELECTRICAL CHARACTERISTICS

Table 20. Absolute Ratings

Parameter	Min.	Typ.	Max.	Note
PVDD			5.6 volts	
CVDD			5.6 volts	
Vin	Vss-0.5 volt		Vcc+0.5V	
Operating temperature	0 degree C		70 degree C	
Storage temperature	-65 degree C		150 degree C	
Maximum power consumption			~2W	

Table 21. DC Electrical Characteristic

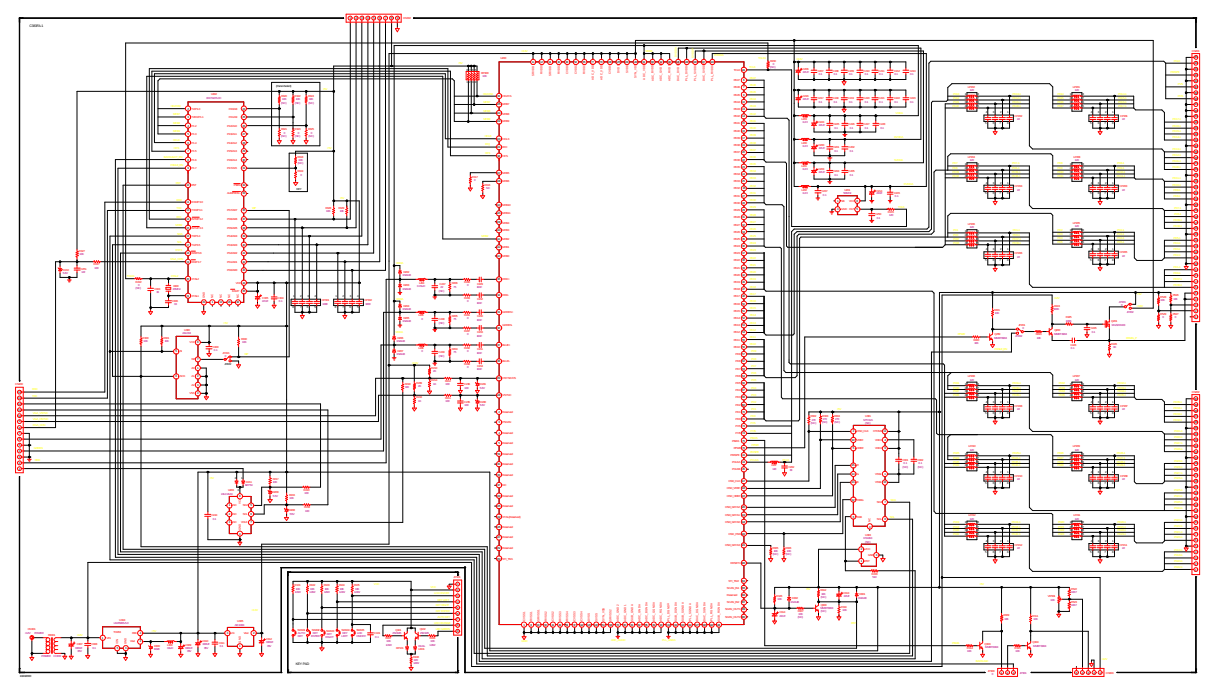
Parameter	Min.	Typ.	Max.	Note
PVDD	3.15 volts	3.3 volts	3.47 volts	
CVDD	3.15 volts	3.3 volts	3.47 volts	
Vil (COMS inputs) Vil (TTL inputs)			0.3*CVDD 0.8 volts	
Vih (COMS inputs) Vih (TTL inputs)	0.7 * CVDD 2.0 volts		1.1*CVDD 5.0+0.5 volts	(1)
Voh	2.4 volts		CVDD	
Vol		0.2 volts	0.4 volts	
Input Current	-10 uA		10 uA	
PVDD operating supply current	0 mA		20 mA/pad @ 10pF	(2)
CVDD operating supply current	0 mA		500 mA	(3)

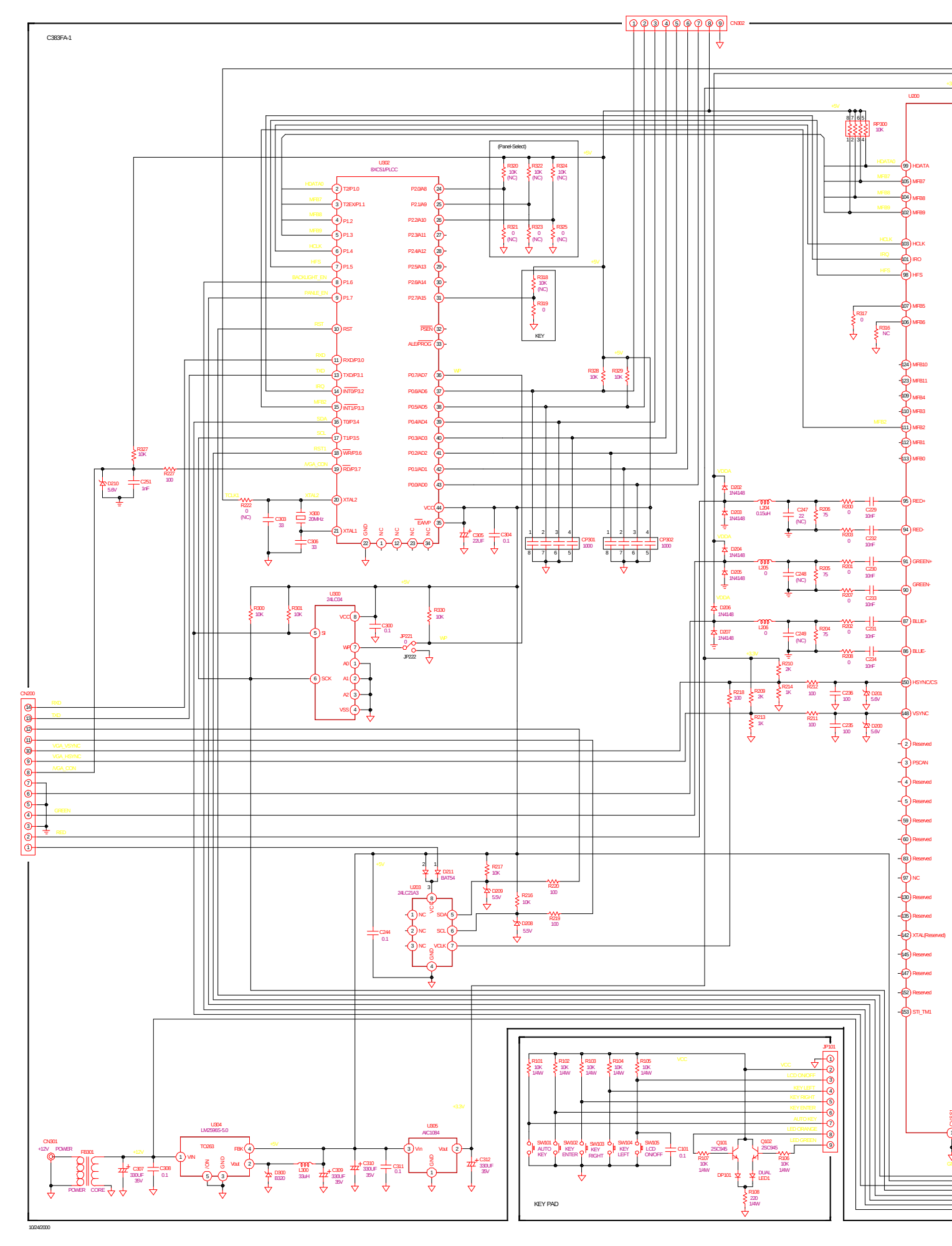
NOTE 1:5V-Tolerent TTL Input pads are as follows:

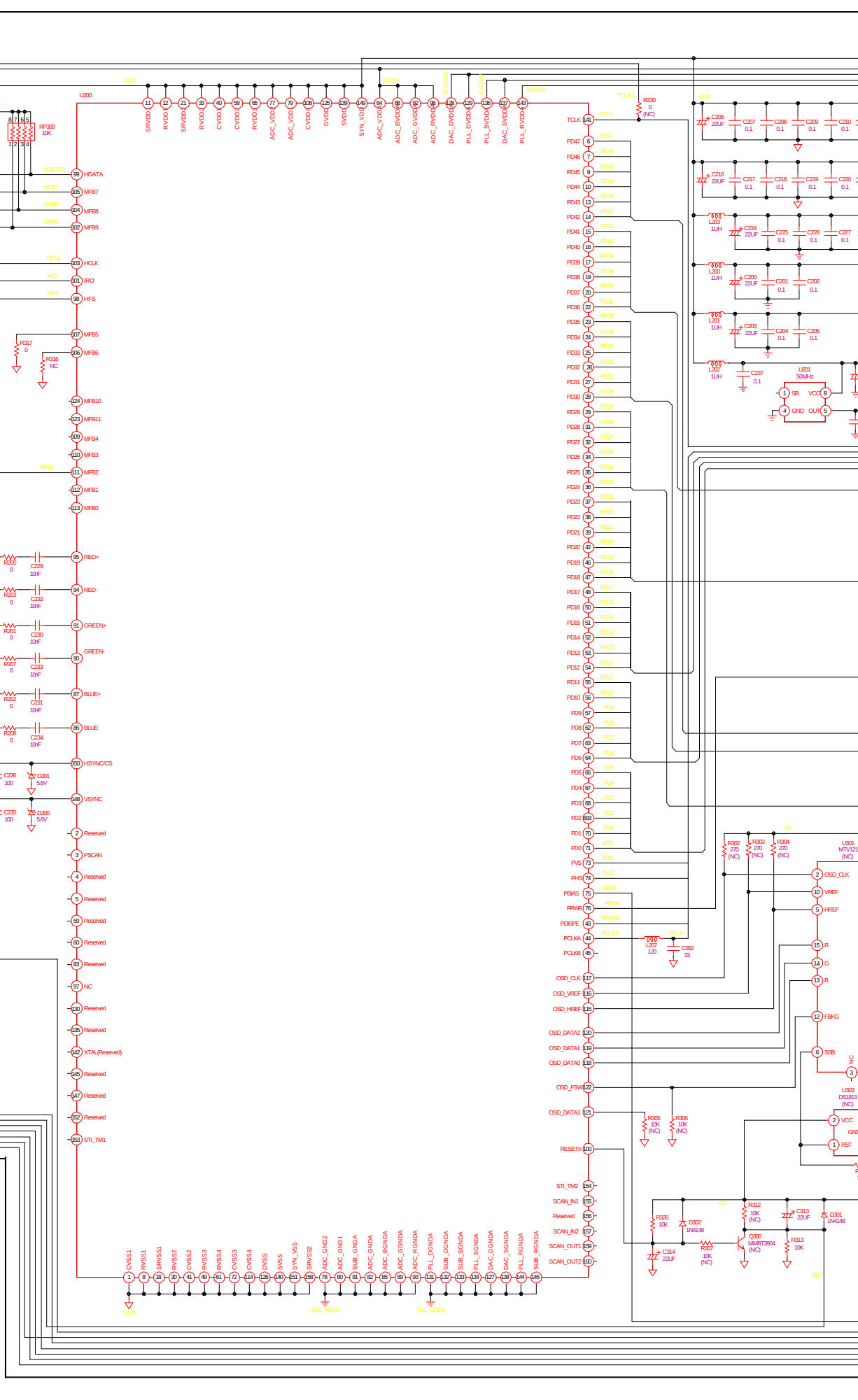
- CRT Interface: HSYNC (pin #150), VSYNC (#148)
- Host Interface: HFS (#98), HCLK (#103), HDATA (#99), RESETN (#100), MFB[11:0]: MFB11 (#123), MFB10 (#124), MFB9 (#102), MFB8 (#104), MFB7 (#105), MFB6 (#106), MFB5 (#107), MFB4 (#109), MFB3 (#110), MFB2 (#111), MFB1 (#112), MFB0 (#113)
- OSD Interface: OSD_DATA3 (#121), OSD_DATA2 (#120), OSD_DATA1 (#119), OSD_DATA0 (#118), OSD_FSW (#122)
- Non-5V-Tolerant TTL Input Pad is: TCLK(#141)

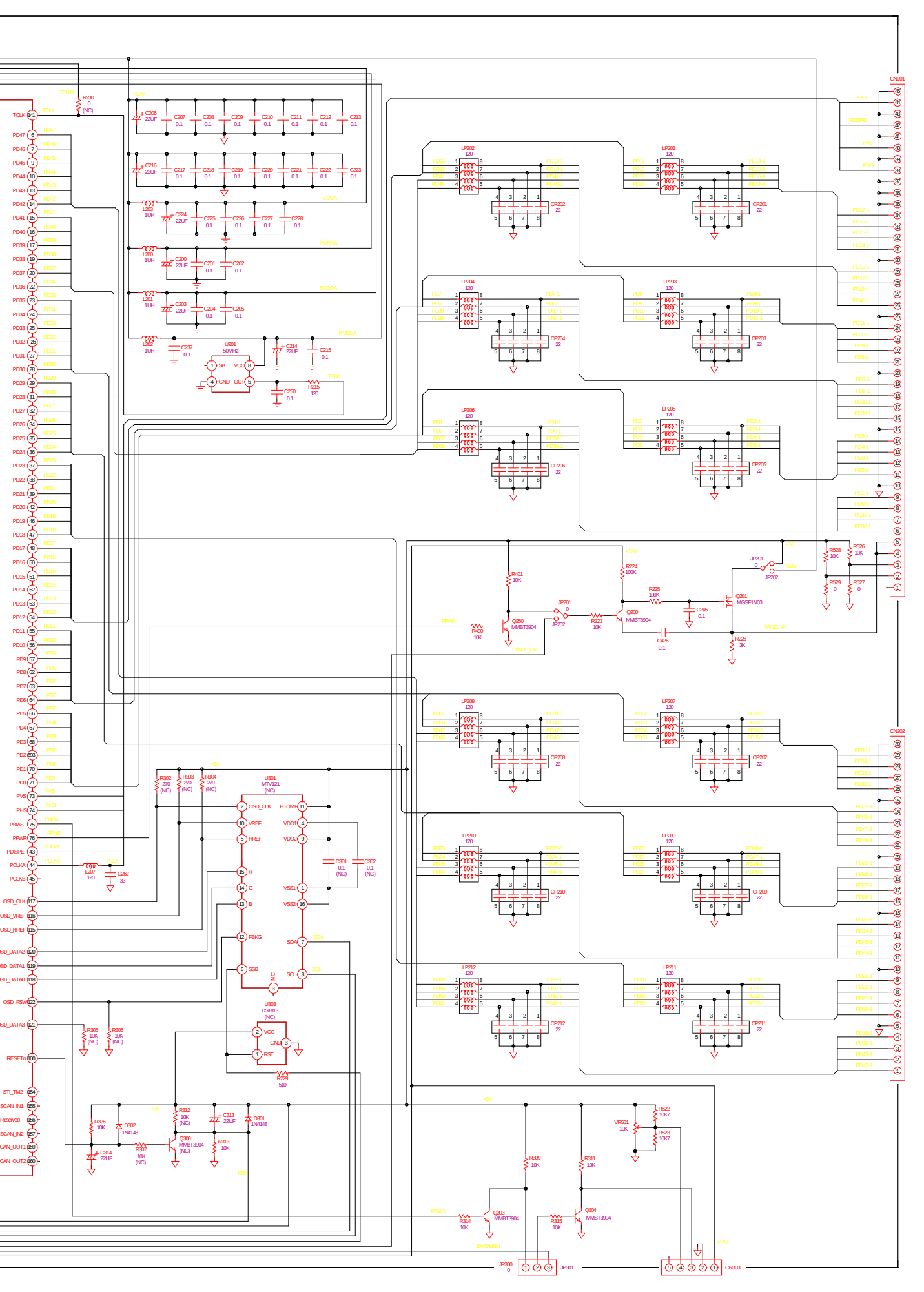
NOTE 2: When the panel interface is disabled, the supply current is 0 mA. The drive current of each pad can be programmed in the range of 2 mA to 20 mA (@capacitive loading = 10 pF)

NOTE 3: When all circuits are powered down and TCLK is stopped, the CVDD supply current becomes 0 mA.




C383FA-1
CN302
U200
U302
8XC51/PLCC
(Panel-Select)
KEY
U800
24LC04
U203
24LC21A/3
U804
LM2596S-5.0
U805
AIC1084
CN200
CN801
JP101
KEY PAD
HDATA
MFB7
MFB8
MFB9
HCLK
IRQ
HFS
MFB5
MFB6
MFB10
MFB11
MFB4
MFB3
MFB2
MFB1
MFB0
RED+
RED-
GREEN+
GREEN-
BLUE+
BLUE-
HSYNC/CS
VSYNC
PSCAN
XTAL(Reserved)
STI_TM1
RXD
TXD
VGA_VSYNC
VGA_HSYNC
VGA_CON
GREEN
RED
HDATA0
MFB7
MFB8
MFB9
HCLK
IRQ
HFS
RST
BACKLIGHT_EN
PANLE_EN
RXD
TXD
IRQ
MFB2
SDA
SCL
RST1
VGA_CON
XTAL2
XTAL1
WP
EAVP
VCC
LCD ON/OFF
KEY LEFT
KEY RIGHT
KEY ENTER
AUTO KEY
LED ORANGE
LED GREEN
+5V
+12V
+3.3V
VDDA
POWER
CORE
FB301
SW601 AUTO KEY
SW602 KEY ENTER
SW603 KEY RIGHT
SW604 KEY LEFT
SW605 LCD ON/OFF
Q101 2SC945
Q102 2SC945
DUAL LED1
DP101
10/24/2000


U200
RP300 10K
HDATA0
MFB7
MFB8
MFB9
HCLK
IRQ
HFS
R317 0
R316 NC
MFB10
MFB11
MFB4
MFB3
MFB2
MFB1
MFB0
R200 0
C229 10nF
R203 0
C232 10nF
R201 0
C230 10nF
R207 0
C233 10nF
R202 0
C231 10nF
R208 0
C234 10nF
C236 100
D201 5.6V
C235 100
D200 5.6V
RED+
RED-
GREEN+
GREEN-
BLUE+
BLUE-
HSYNC/CS
VSYNC
Reserved
PSCAN
XTAL(Reserved)
STI_TM1
TCLK
PD47
PD46
PD45
PD44
PD43
PD42
PD41
PD40
PD39
PD38
PD37
PD36
PD35
PD34
PD33
PD32
PD31
PD30
PD29
PD28
PD27
PD26
PD25
PD24
PD23
PD22
PD21
PD20
PD19
PD18
PD17
PD16
PD15
PD14
PD13
PD12
PD11
PD10
PD9
PD8
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
PVS
PHS
PBIAS
PDWR
PDSPE
PCLKA
PCLKB
OSD_CLK
OSD_VREF
OSD_HREF
OSD_DATA2
OSD_DATA1
OSD_DATA0
OSD_FSW
OSD_DATA3
RESETn
STI_TM2
SCAN_IN1
Reserved
SCAN_IN2
SCAN_OUT1
SCAN_OUT2
TCLK1
R230 0 (NC)
C206 22UF
C207 0.1
C208 0.1
C209 0.1
C210 0.1
C216 22UF
C217 0.1
C218 0.1
C219 0.1
C220 0.1
L203 1UH
C224 22UF
C225 0.1
C226 0.1
C227 0.1
L200 1UH
C200 22UF
C201 0.1
C202 0.1
L201 1UH
C209 22UF
C204 0.1
C205 0.1
L202 1UH
C237 0.1
U201 50MHz
SB
VCC
GND
OUT
PCLK
L207 120
C262 33
R302 270 (NC)
R303 270 (NC)
R304 270 (NC)
U301 MTV121 (NC)
R305 10K (NC)
R306 10K (NC)
U303 DS1813 (NC)
VCC
RST
GND
R326 10K
D302 1N4148
R307 10K (NC)
C314 22UF
R312 10K (NC)
C313 22UF
D301 1N4148
Q300 MMBT3904 (NC)
R313 10K
RST
CVSS1
RVSS1
SRVSS1
RVSS2
CVSS2
RVSS3
RVSS4
CVSS3
CVSS4
DVSS
SVSS
SYN_VSS
SRVSS2
ADC_GND2
ADC_GND1
SUB_GNDA
ADC_GNDA
ADC_BGNDA
ADC_GGNDA
ADC_RGNDA
PLL_DGNDA
SUB_DGNDA
SUB_SGNDA
PLL_SGNDA
DAC_DGNDA
DAC_SGNDA
PLL_RGNDA
SUB_RGNDA
GND
ADC_AGND
PLL_GNDA


TCLK
R230 0 (NC)
+3.3V
C206 22UF
C207 0.1
C208 0.1
C209 0.1
C210 0.1
C211 0.1
C212 0.1
C213 0.1
C216 22UF
C217 0.1
C218 0.1
C219 0.1
C220 0.1
C221 0.1
C222 0.1
C223 0.1
VDDA
L203 1UH
C224 22UF
C225 0.1
C226 0.1
C227 0.1
C228 0.1
DVDDA
L200 1UH
C200 22UF
C201 0.1
C202 0.1
SVDDA
L201 1UH
C203 22UF
C204 0.1
C205 0.1
RVDDA
L202 1UH
C237 0.1
U201 50MHz
SB
VCC
GND
OUT
C214 22UF
C215 0.1
C250 0.1
RZ15 120
CN201
PCLK
PDISPE
PVS
PHS
LP202 120
LP201 120
LP204 120
LP203 120
LP206 120
LP205 120
CP202 22
CP201 22
CP204 22
CP203 22
CP206 22
CP205 22
R401 10K
R224 100K
R225 100K
JP201 0
JP202
Q250 MMBT3904
Q200 MMBT3904
Q001 MGSF1N03
R400 10K
R223 10K
C245 0.1
C425 0.1
R226 3K
R528 10K
R526 10K
R529 0
R527 0
PPWR
PANLE_EN
PANEL_P
+5V
+12V
+3.3V
CN202
LP208 120
LP207 120
LP210 120
LP209 120
LP212 120
LP211 120
CP208 22
CP207 22
CP210 22
CP209 22
CP212 22
CP211 22
U001 MTV121 (NC)
R302 270 (NC)
R303 270 (NC)
R304 270 (NC)
OSD_CLK
VREF
HREF
R
G
B
FBKG
SSB
HTOME
VDD1
VDD2
VSS1
VSS2
SDA
SCL
NC
C301 0.1 (NC)
C302 0.1 (NC)
L207 120
C262 33
U303 DS1813 (NC)
VCC
GND
RST
R305 10K (NC)
R306 10K (NC)
R229 510
R226 10K
D302 1N4148
R312 10K (NC)
C313 22UF
D301 1N4148
C314 22UF
R307 10K (NC)
Q300 MMBT3904 (NC)
R313 10K
RST
R309 10K
R311 10K
VR501 10K
R522 10K7
R523 10K7
PBIAS
R314 10K
R315 10K
Q303 MMBT3904
Q304 MMBT3904
BACKLIGH
JP300 0
JP301
CN303